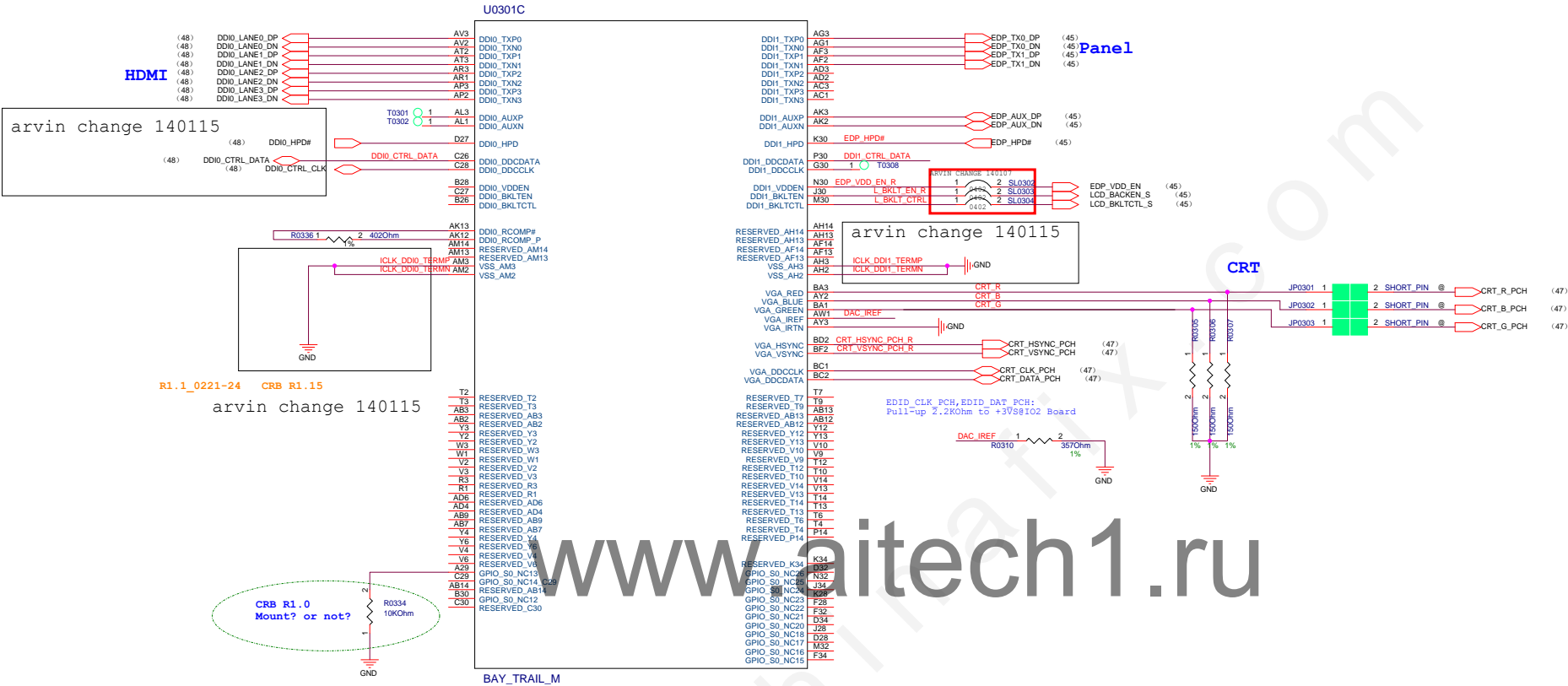


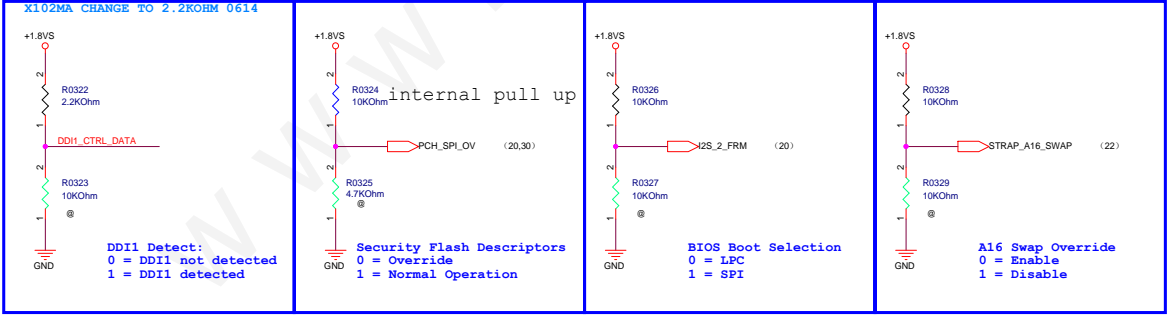
SKU Table

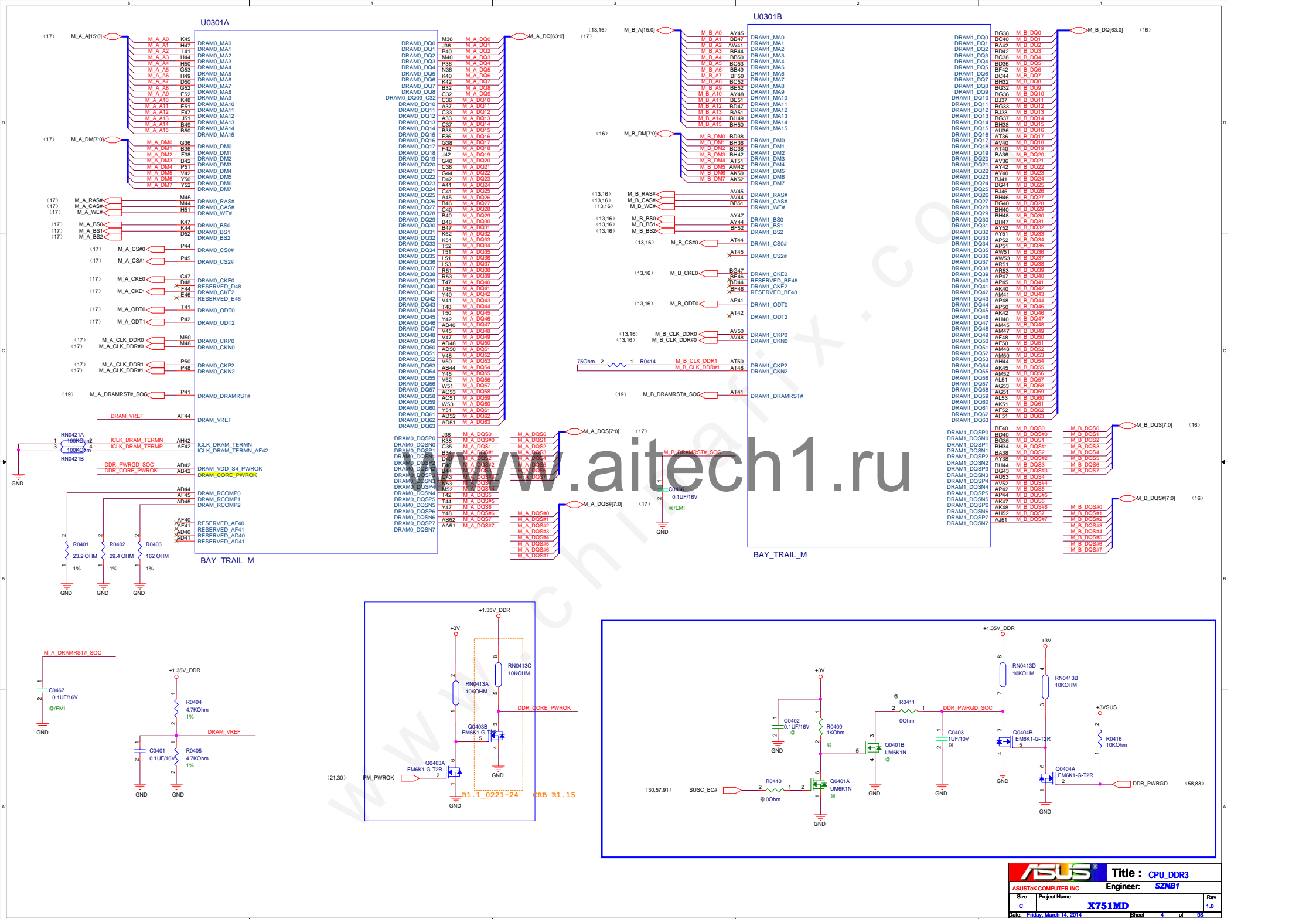
	CPU	DIMM	USB3/USB2	TV	3G	VRAM	BT	HDMI	2D/3D	TPM	PCH	DRAM	VRAM
Option	/CPU	/DIMM	/USB3; /USB2	/TV	/3G	/VRAM	/BT	/HDMI	/2D; /3D	/TPM	/PCH		
60NB06P0-MB1110	N3530	4G_KINGSTON	-	-	-	-	-	-	-	-	-	4G HYNIX	V2G-MICRON
60NB06P0-MB1500	N2830	4G_SAMSUNG	-	-	-	-	-	-	-	-	-	4G MICRON	V2G-HYNIX
60NB06P0-MB1600	N2830	4G_HYX	-	-	-	-	-	-	-	-	-	4G HYNIX	V1G-SAMSUNG
60NB06P0-MB1700	N2930	2G_HYN	-	-	-	-	-	-	-	-	-	0M	V1G-HYNIX

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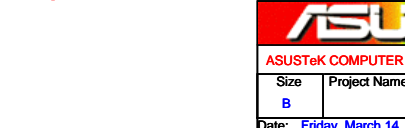
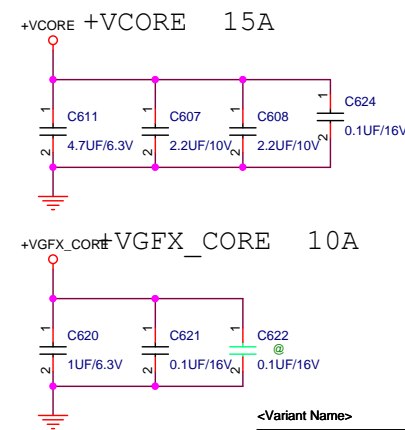
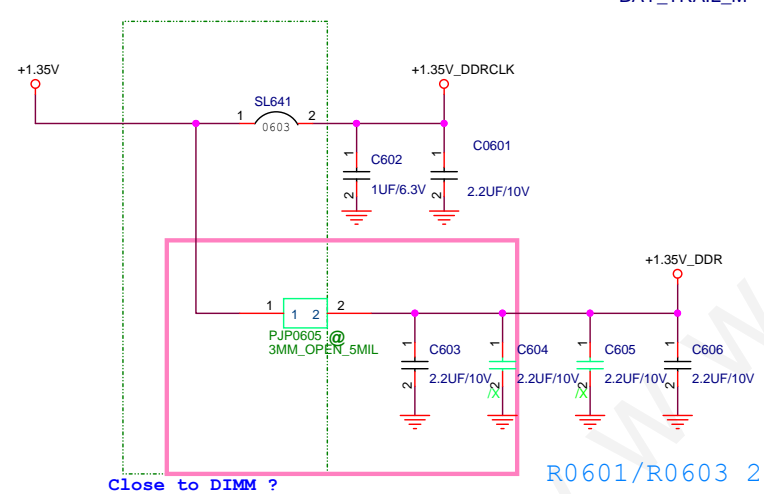
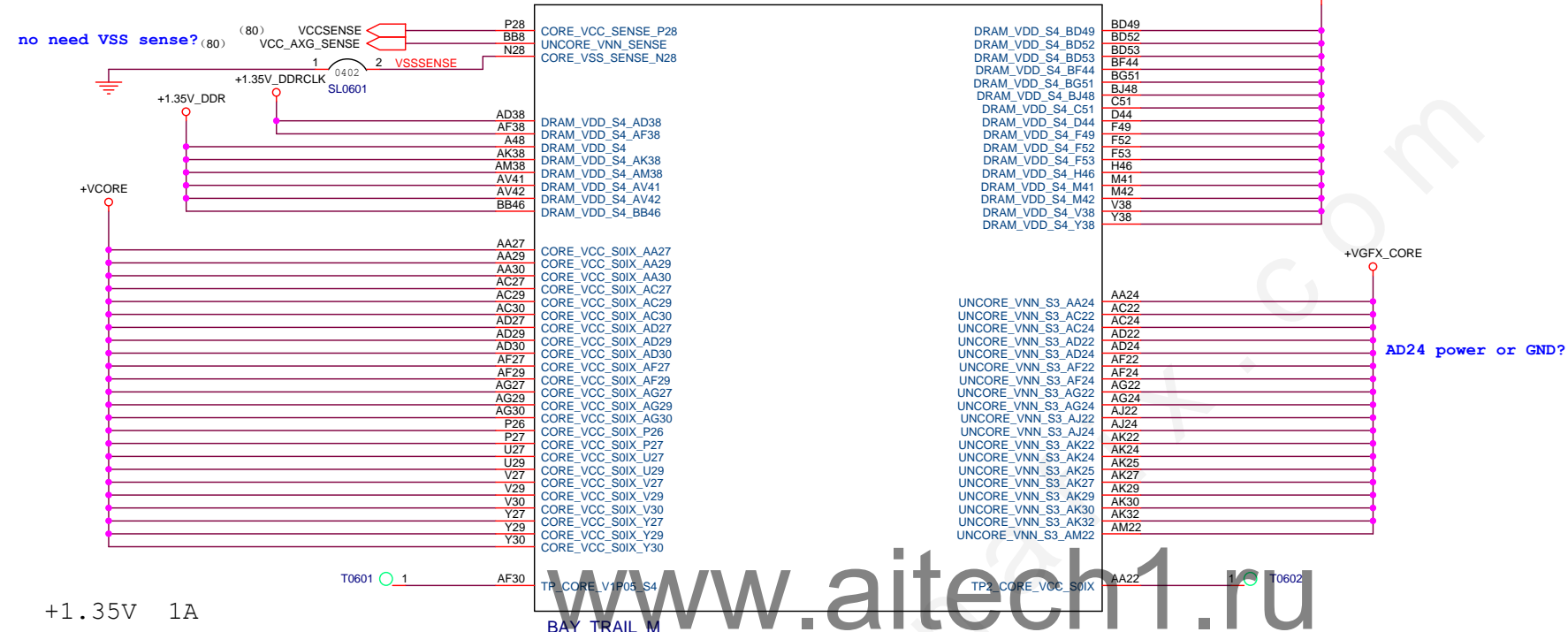
Straps






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U0301G



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		Title : XDP Debug Board	
ASUSTeK COMPUTER INC. NB3		Engineer: RD1_EE2-1	
Size B	Project Name S200T_Bay Trail-M		Rev 1.0
Date: Friday, March 14, 2014		Sheet 7 of 98	

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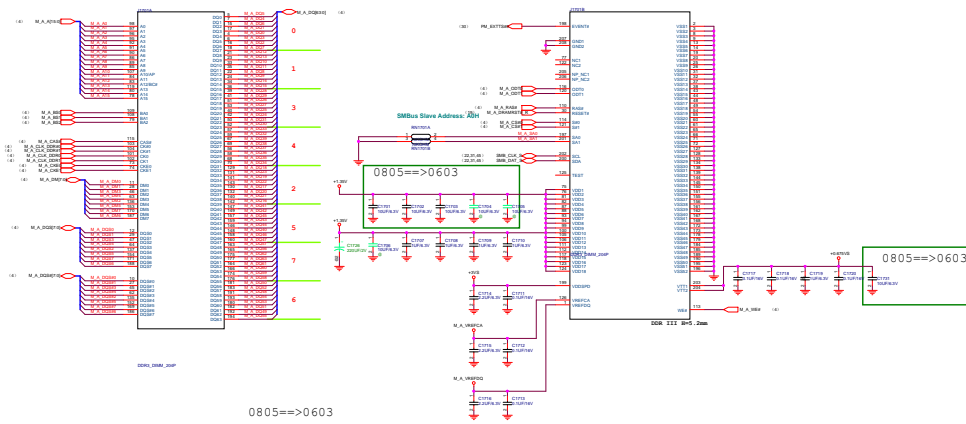
www.aitech1.ru

		Title : NB_****	
ASUSTeK COMPUTER INC.		Engineer: RD1_EE2-1	
Size	Project Name		Rev
C	S200T Bay Trail-M		1.0
Date: Friday, March 14, 2014		Sheet	12 of 95

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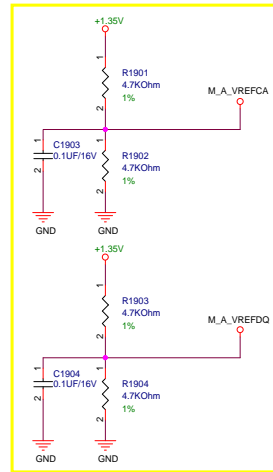
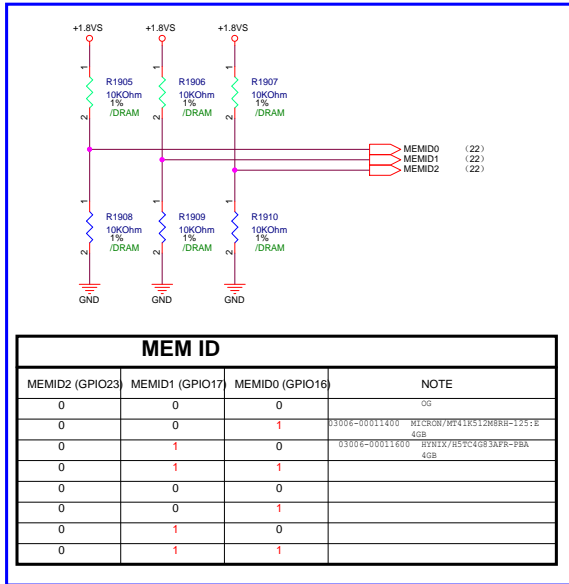


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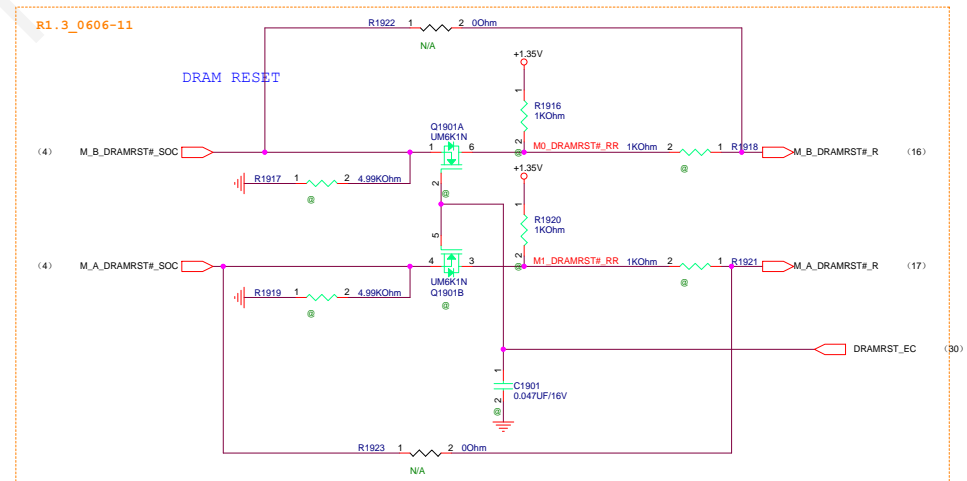
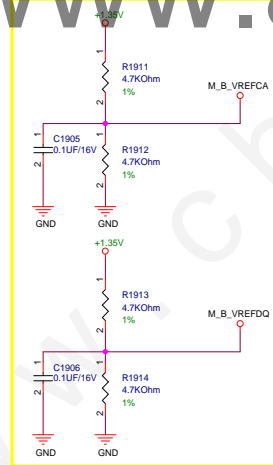
Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details

DDR3 Vref

Intel Document Number: 400755



Near DIMM Device <5000 mil



arvin change 140116

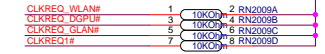
follow X550LD arvin 140107

follow X751MD 13/31

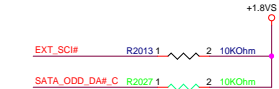
U0301D

X552MD

X550MD MODIFY 13/31



X552MD



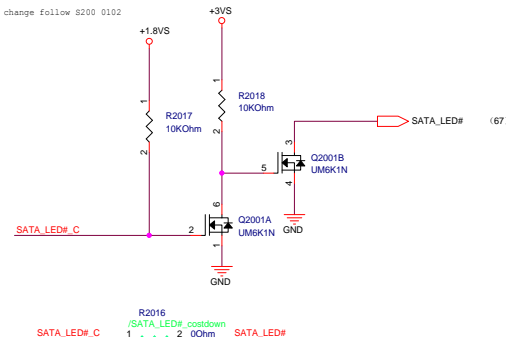
X552MD



R1.2_0418-7

BAY_TRAIL_M

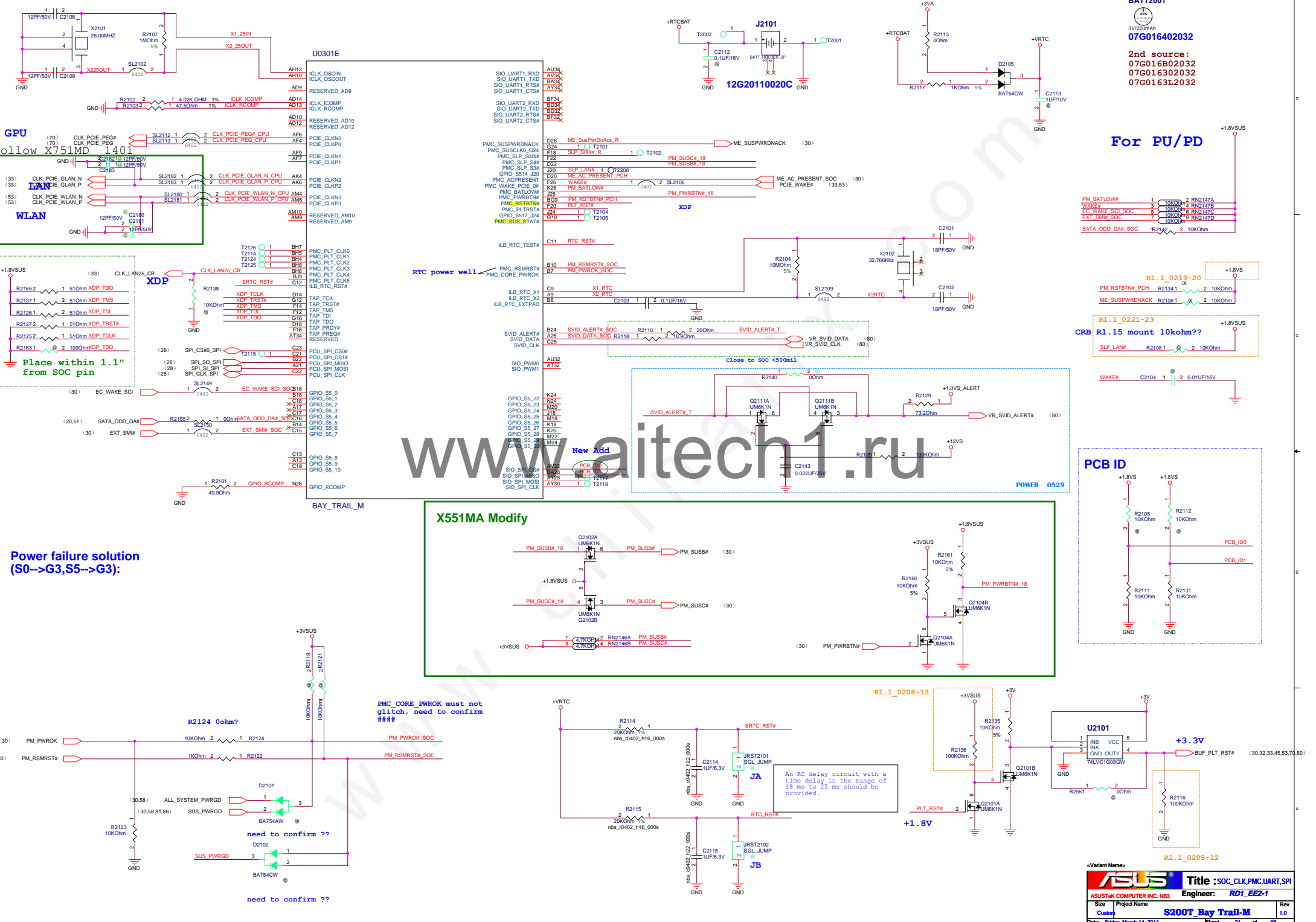
arvin change follow S200 0102



R1.1_0221-24 CRB R1.15

BOB

RTC Connector



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<Variant Name>



Title : CPU_PCIE,USB

ASUSTeK COMPUTER INC. NB3

Engineer: RD1_EE2-1

Size
B

Project Name

S200T_Bay Trail-M


Rev
1.0

Date: Friday, March 14, 2014

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BOM



Title : CPU_PCHCLOCK SIGNALS

ASUSTeK COMPUTER INC. NB1

Engineer: RD1_EE2-1

Size	Project Name	Rev
B	S200T_Bay Trail-M	1.0

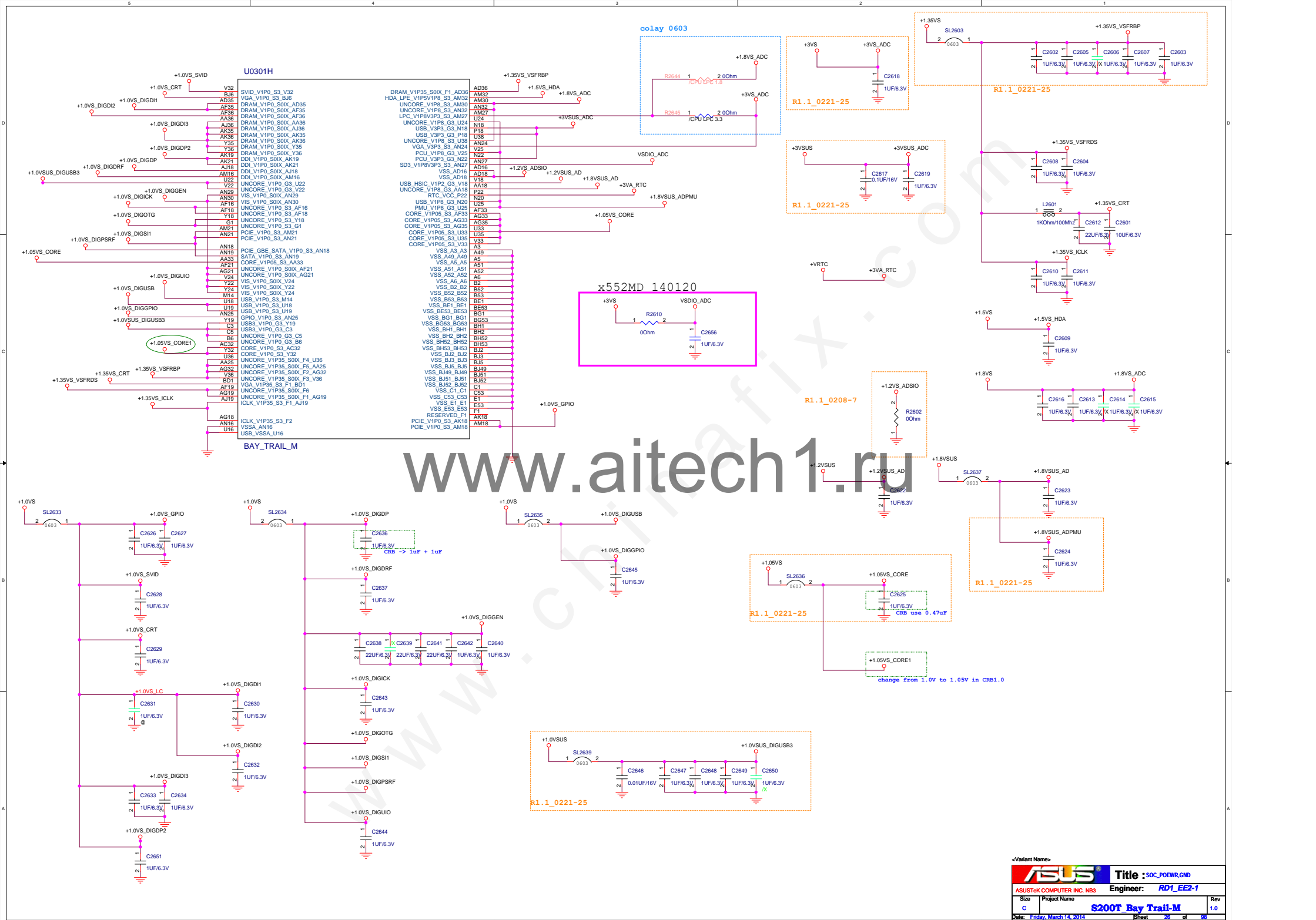
Date: Friday, March 14, 2014

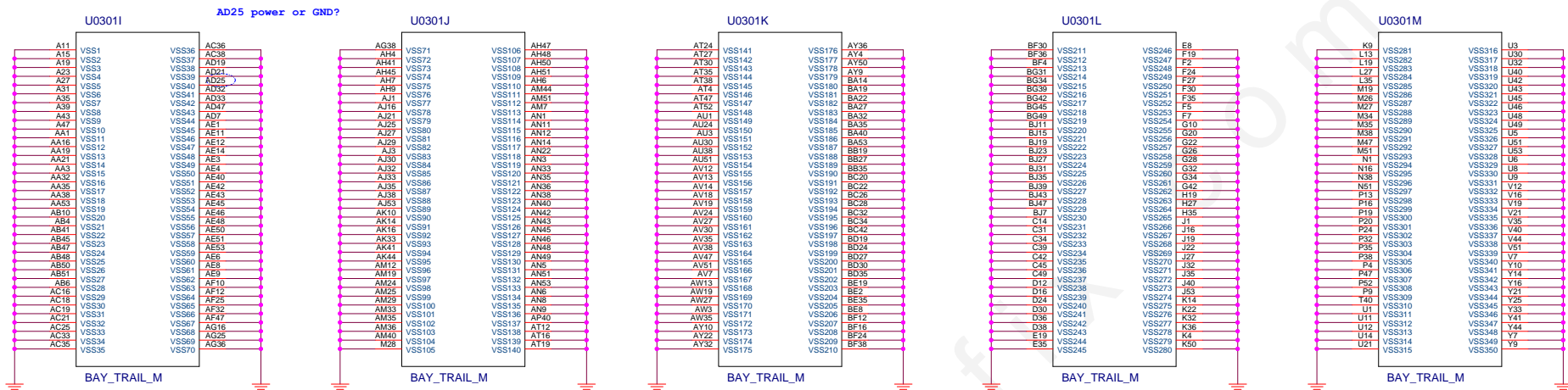
Sheet 24 of 98

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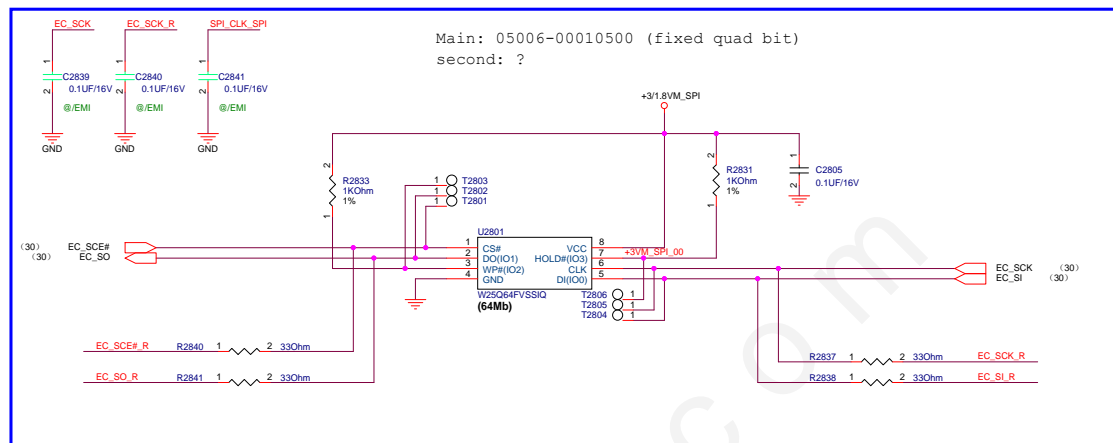
BOM

		Title : CPU_PCH_SYS_POWER	
ASUSTeK COMPUTER INC. NB1		Engineer: RD1_EE2-1	
Size	Project Name		Rev
Custom	S200T_Bay Trail-M		1.0
Date: Friday, March 14, 2014		Sheet	25 of 98



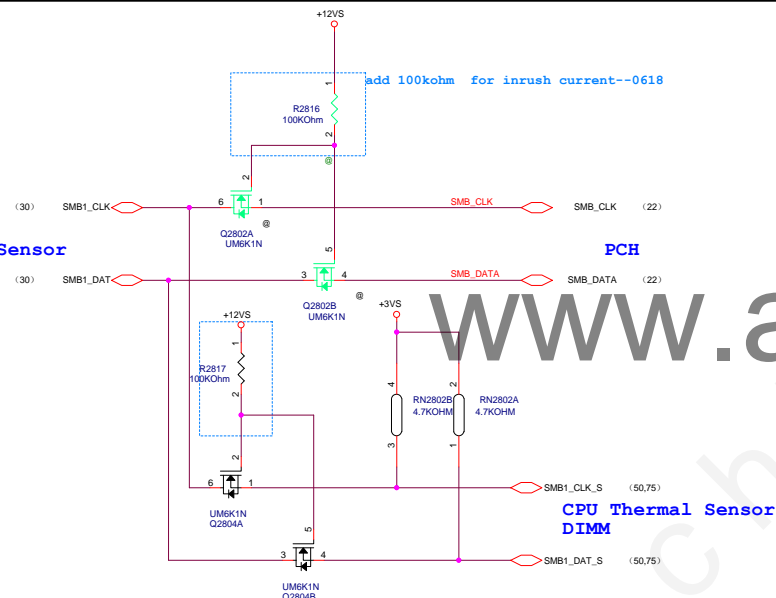


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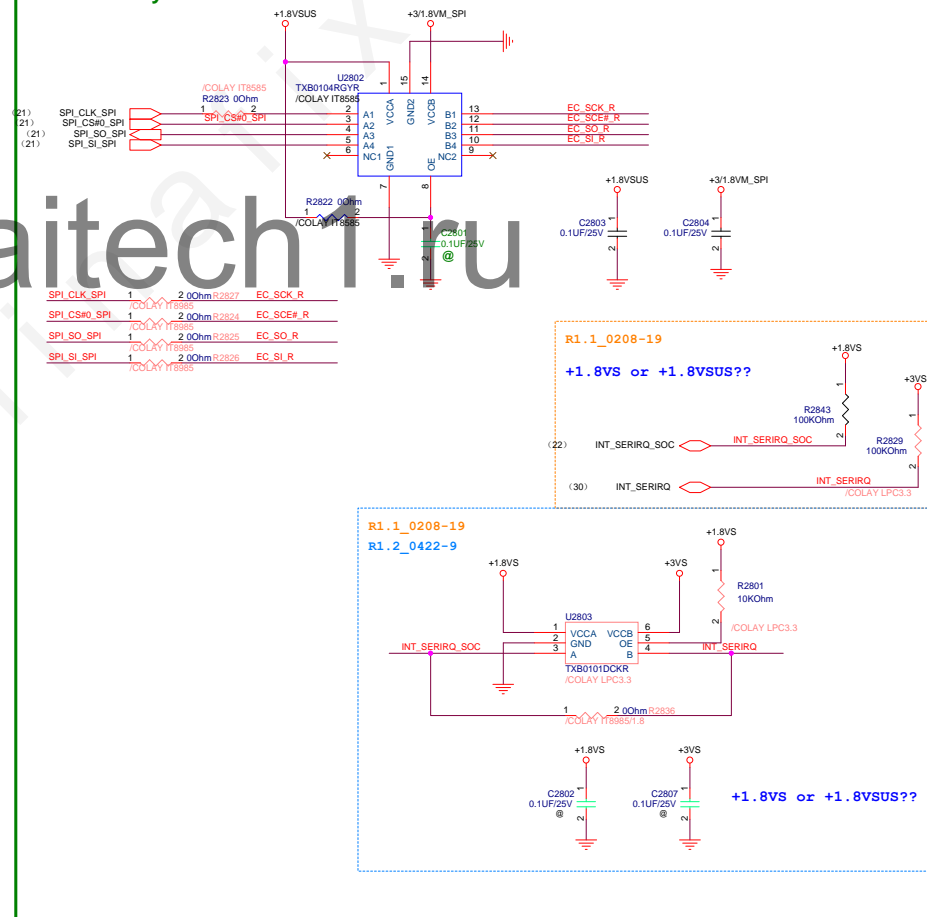


EC (30) S

CPU/ GPU Thermal Sensor



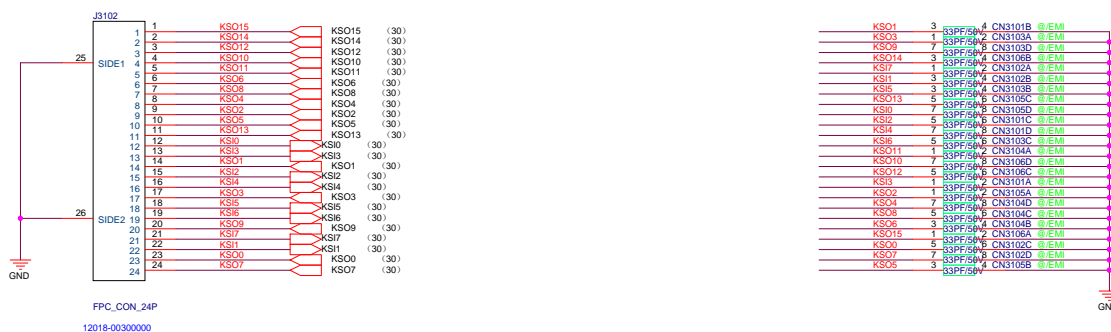
+1.8VS or +1.8VSUS??



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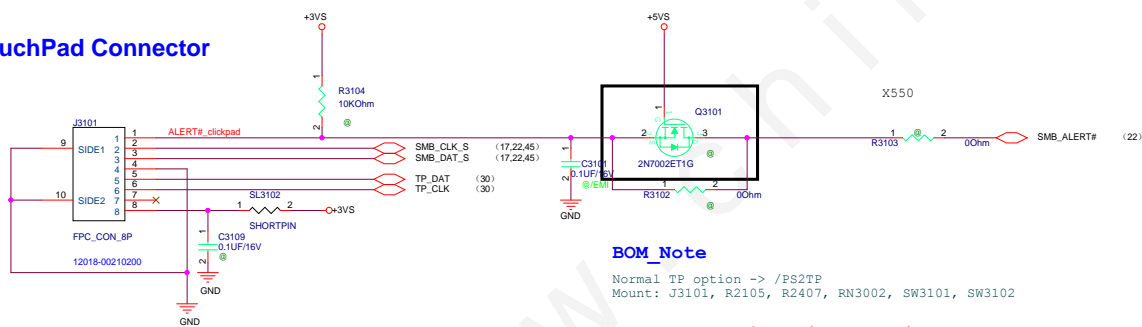
Note
Only 3V Tolerance
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GPR[

Keyboard Connector



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TouchPad Connector



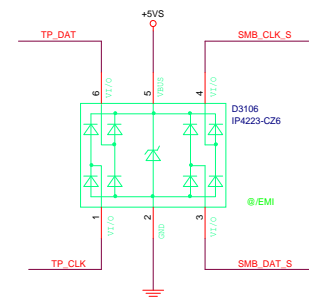
BOM_Note

Normal TP option -> /PS2TP
Mount: J3101, R2105, R2407, RN3002, SW3101, SW3102

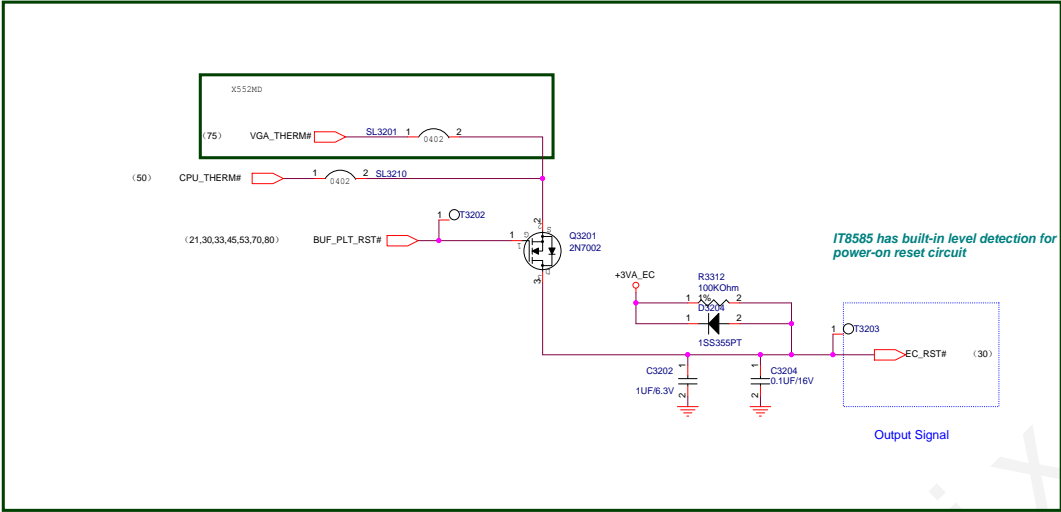
ELAN SMBUS TP option -> /ELAN PAD + /CPAD
Mount: R2106, R2408, RN3008, Q3I02, J3104

Synaptics SMBUS TP option -> /CPAD
Mount: J3104, R2408, RN3008

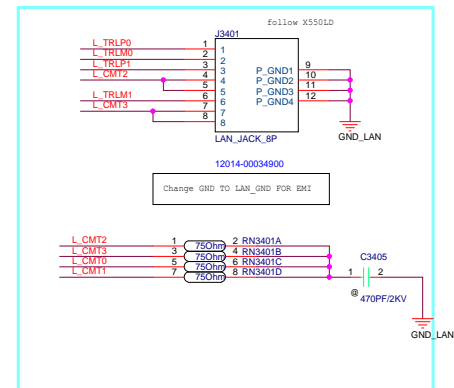
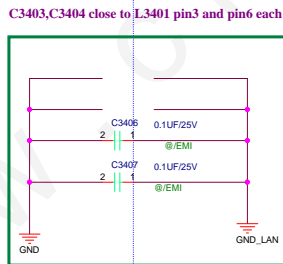
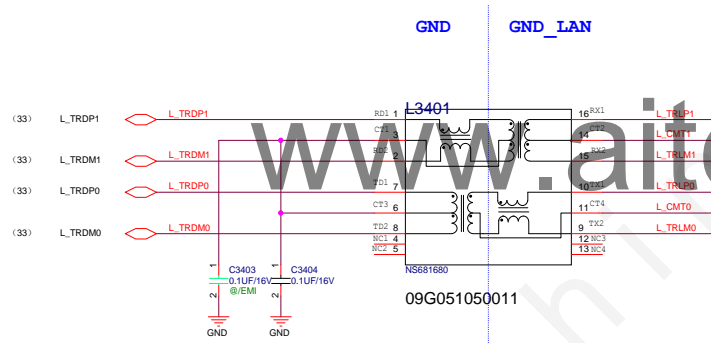
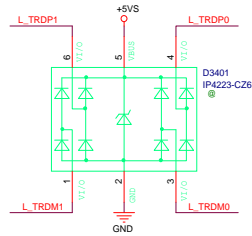
Reserved for EMI



<Variant Name>




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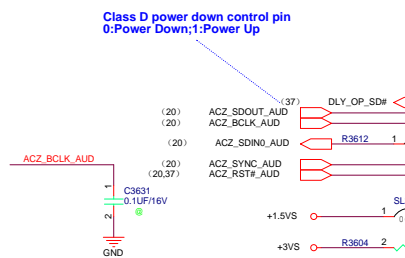
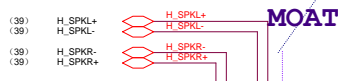
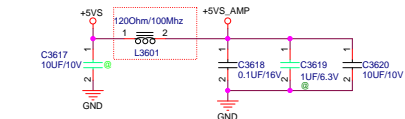
<Variant Name>

		Title : SERIAL PORT	
ASUSTeK COMPUTER INC. NB1		Engineer: RD1_EE2-1	
Size	Project Name	Rev	
Custom	X102MA_Bay Trail-M	1.0	
Date: Friday, March 14, 2014		Sheet	35 of 98

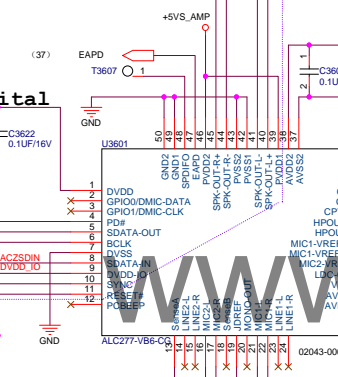
DIGITAL

MOAT

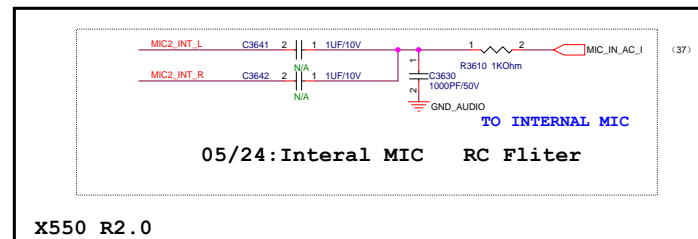
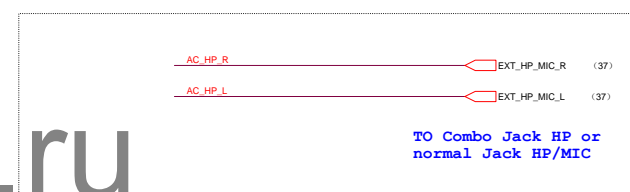
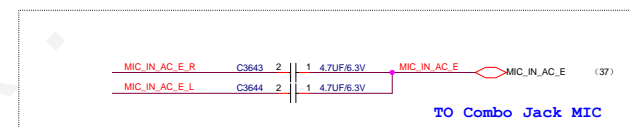
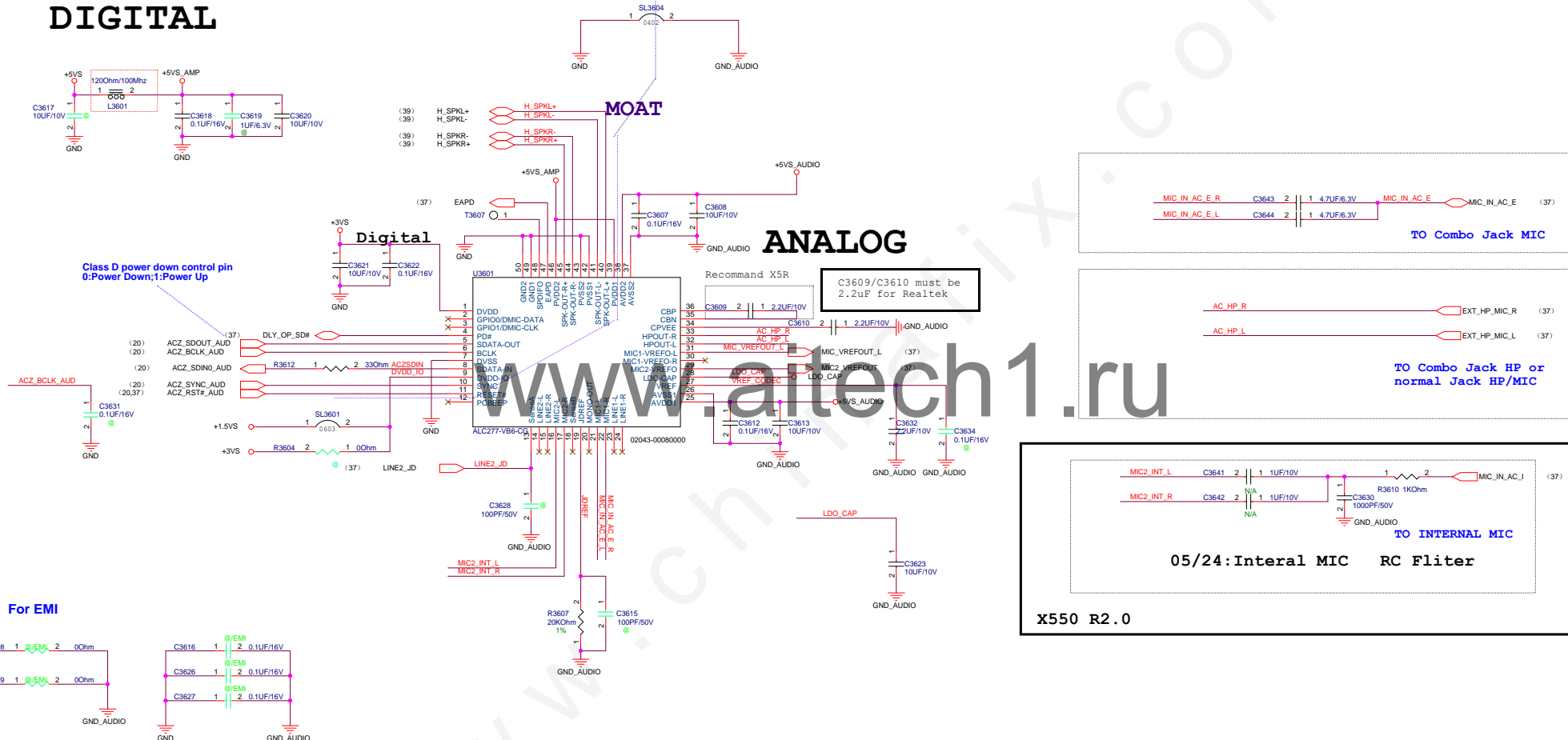
ANALOG

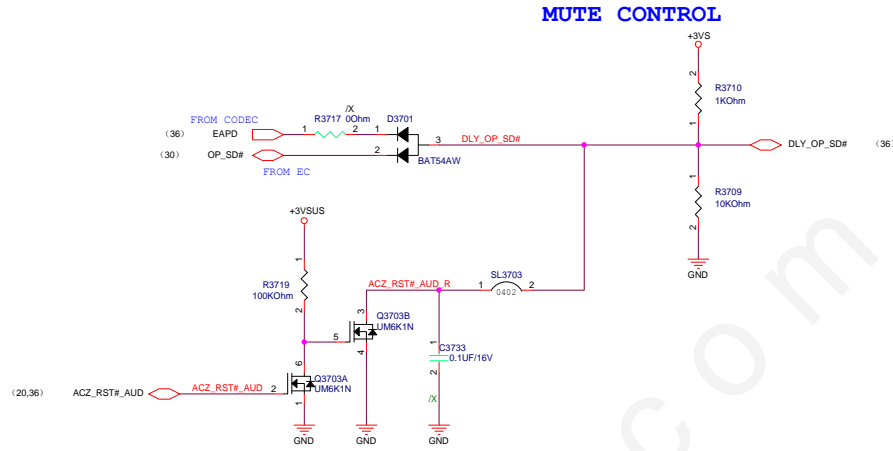
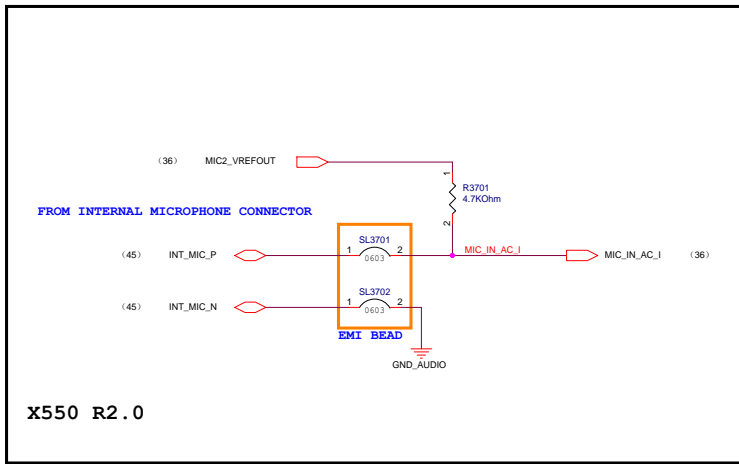


Digital

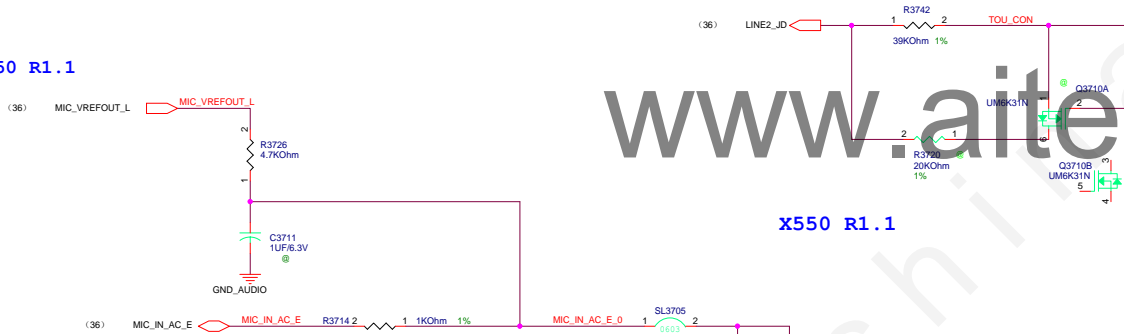


For EMI

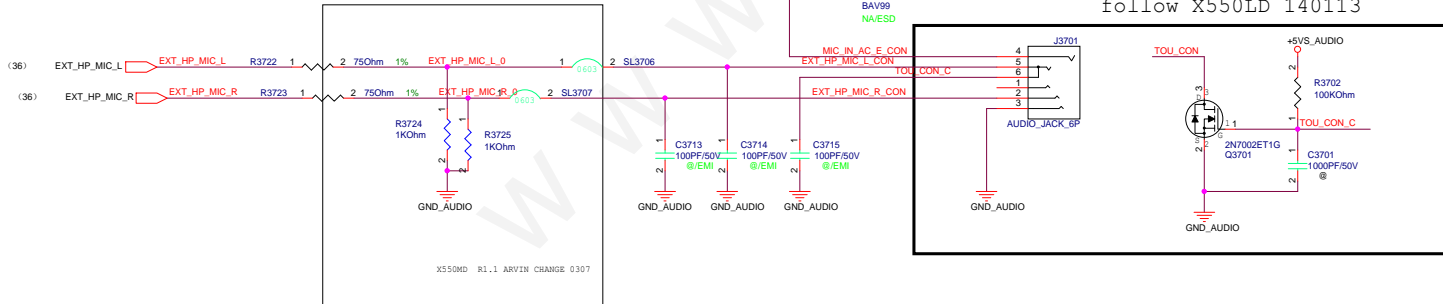




X550 R1.1



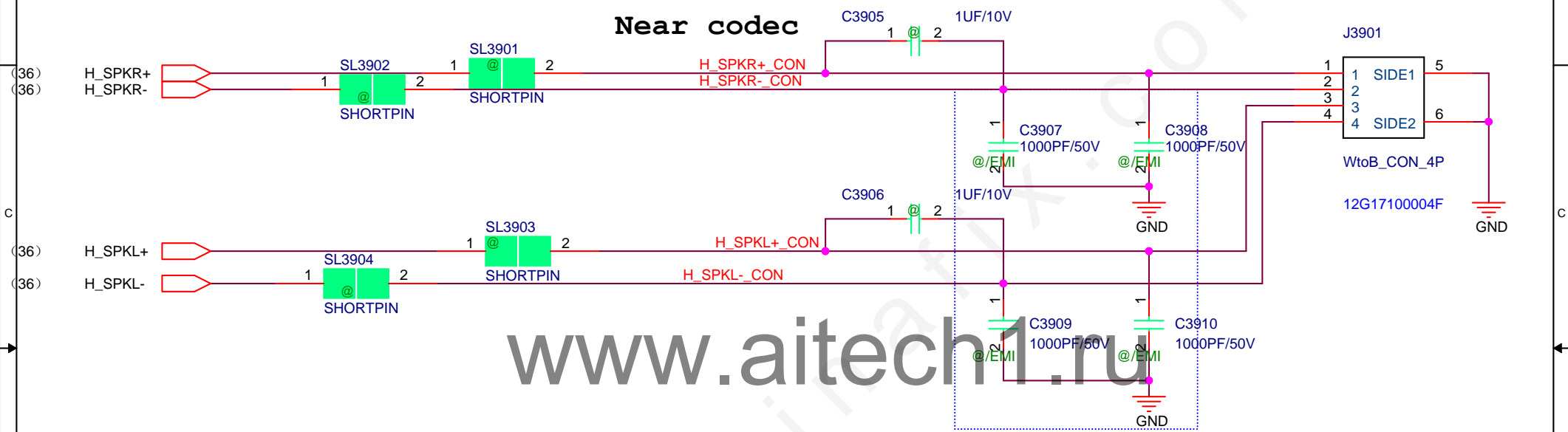
X550 R1.1



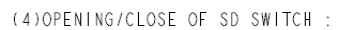
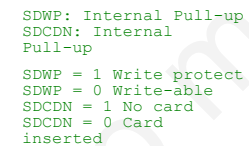
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<Variant Name>		Title : ****	
ASUS		Engineer: SZ_SYS2	
Size	Project Name	Rev	
C	X551CA	1.0	
Date: Friday, March 14, 2014		Sheet 38 of 85	

Audio Speaker



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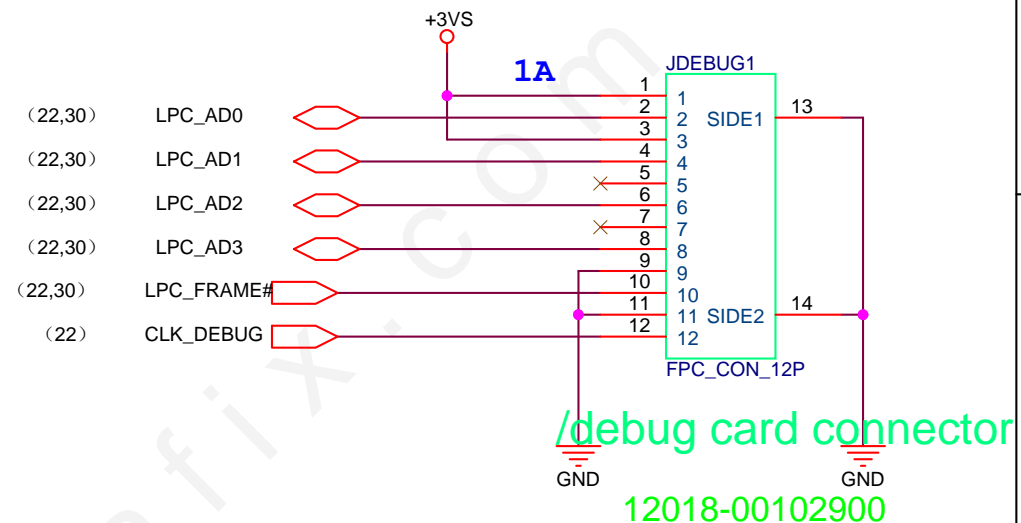
	PROTECT CONTACT		DETECT CONTACT
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	CLOSE	CLOSE	CLOSE
CARD HALF INSERTION	OPEN	OPEN	CLOSE
CARD INSERTION	CLOSE	OPEN	OPEN

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<Variant Name>			Title : ****	
ASUS			Engineer: SZ_SYS2	
Size	Project Name			Rev
C	X551CA			1.0
Date: Friday, March 14, 2014		Sheet 43 of 88		

LPC DEBUG PORT



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LPC DEBUG PORT


TPM interface signals

LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
+3V

LPCPD#
INT_SERIRQ
BUF_PLT_RST#
CLK_33M_TPM
TPM_CLKRUN#
+3VS

		Title :DEBUG PORT	
ASUSTeK COMPUTER INC.		Engineer: SZ_SYS2	
Size A	Project Name X551CA		Rev 1.0
Date: Friday, March 14, 2014		Sheet 44 of 98	

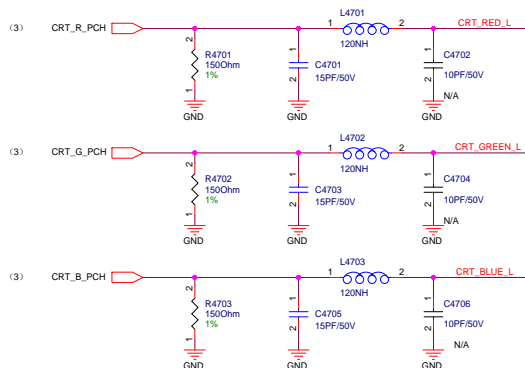
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		Title : ****	
ASUSTeK COMPUTER INC.		Engineer: RD1_EE2-1	
Size A	Project Name X102MA_Bay Trail-M		Rev 1.0
Date: Friday, March 14, 2014		Sheet	46 of 98

DAC Signal

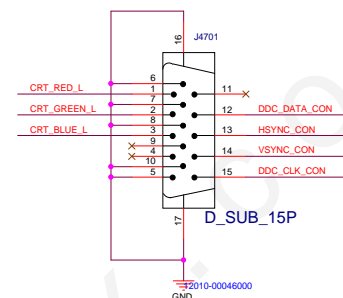
2nd source:
09G023152003
09G023152202
09G023152500

BOM Mount: 09G023152401



follow X550LD

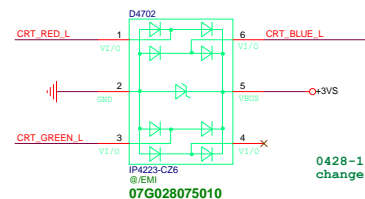
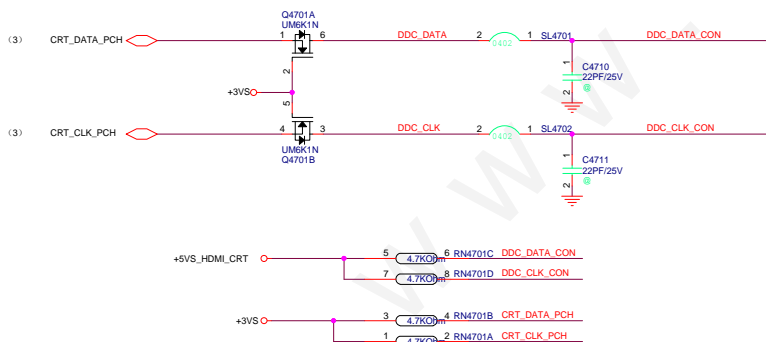
CRT Connector



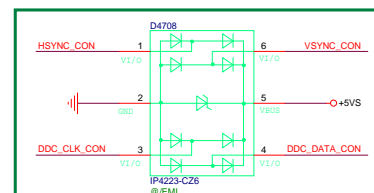
SYNC Signal



Control Signal

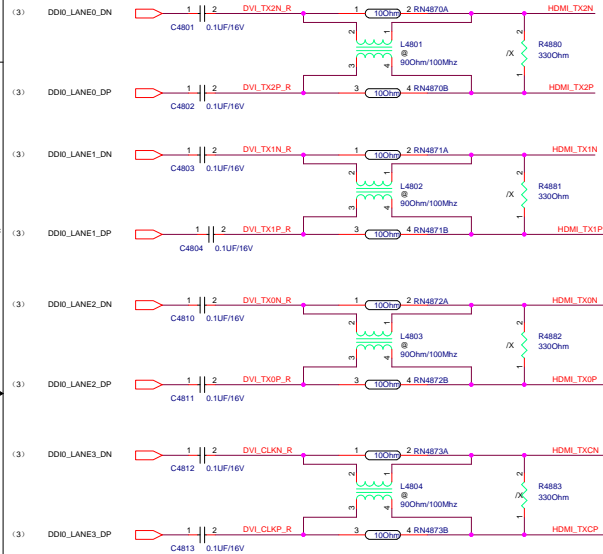


0428-1 EMI D3401, D3402, D4702, D5201, PD6001
change P/N to 07G028176010

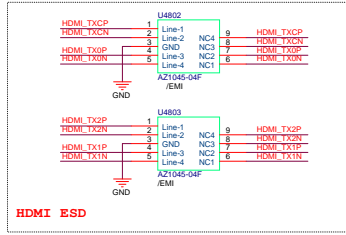


Close to CONNECTOR

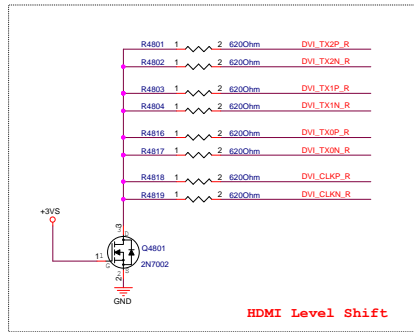
Near CON J4801



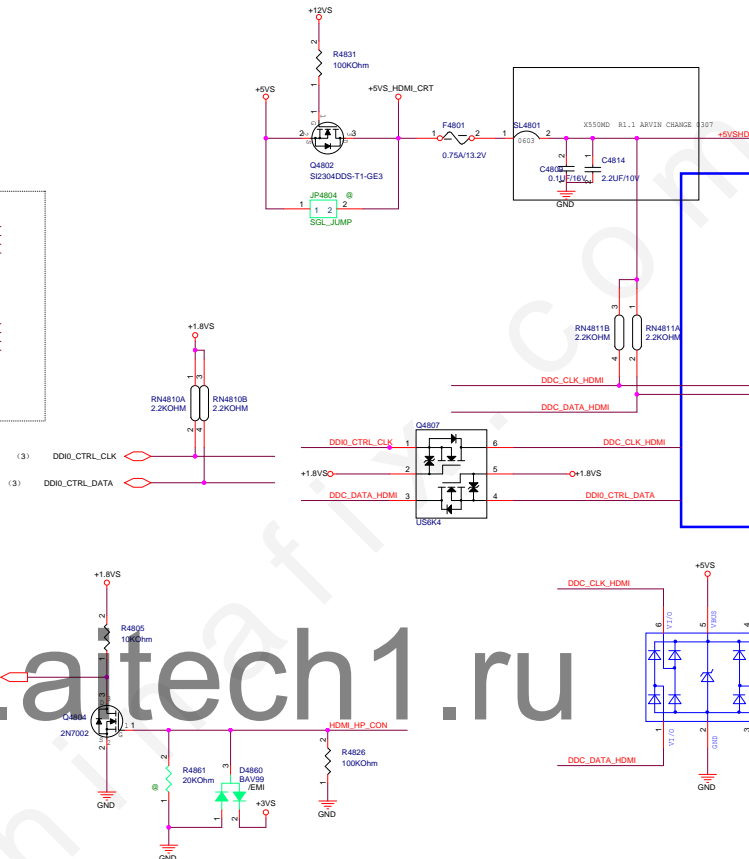
X552MD 01202100



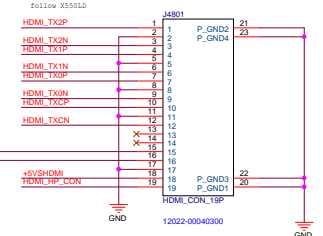
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HDMI Level Shift




HDMI CON.



BOM		Title : HDMI-type D	
ASUSTek COMPUTER INC		Engineer: RDT_EE2-1	
Site	Project Name	Rev	
Custom	S200T_Bay Trail-M	1.0	
Date: Friday, March 14, 2014		Sheet 48 of 98	

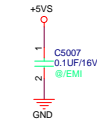
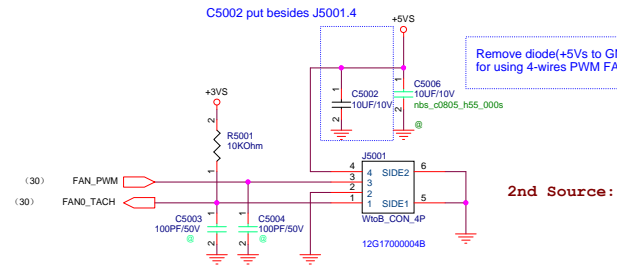
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BOM

		Title : ****
ASUSTeK COMPUTER INC		Engineer: RD1_EE2-1
Size B	Project Name X102MA_Bay Trail-M	Rev 1.0
Date: Friday, March 14, 2014		Sheet 49 of 98

GPU Thermal Sensor

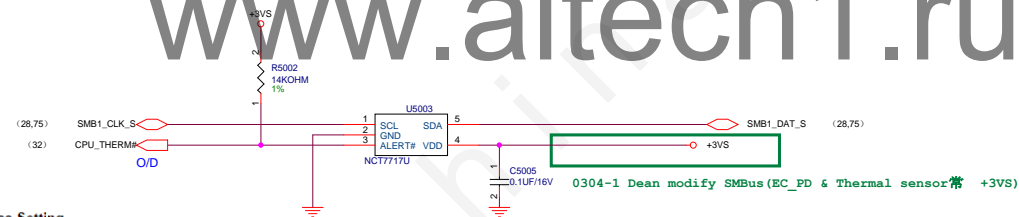
PWM Fan



CPU Thermal Sensor

R5002:14Kohm-->2Kohm

Baytrail Tj,max = 75degC (reason: Tj-sdp = 80degC)



5.3 Address Setting

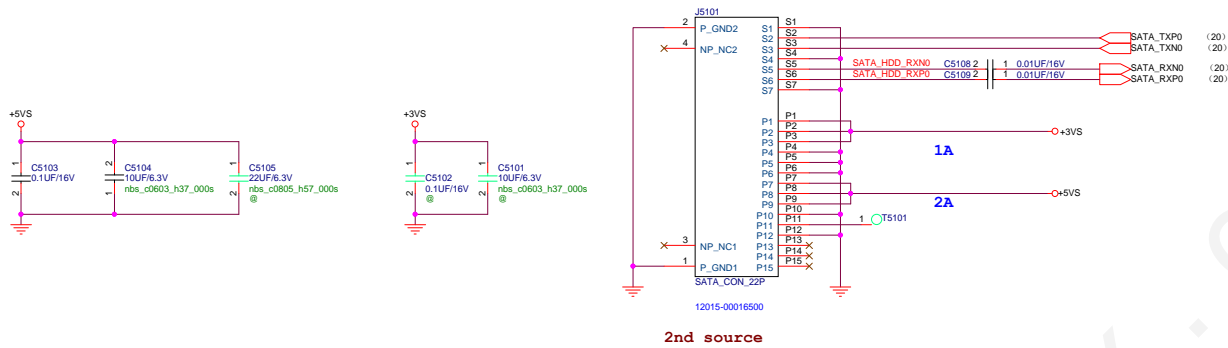
NCT7717U I2C/SMBus address is 1001000xb (x is RW bit).

5.6 ALERT# point hardware power-on setting (TBD)

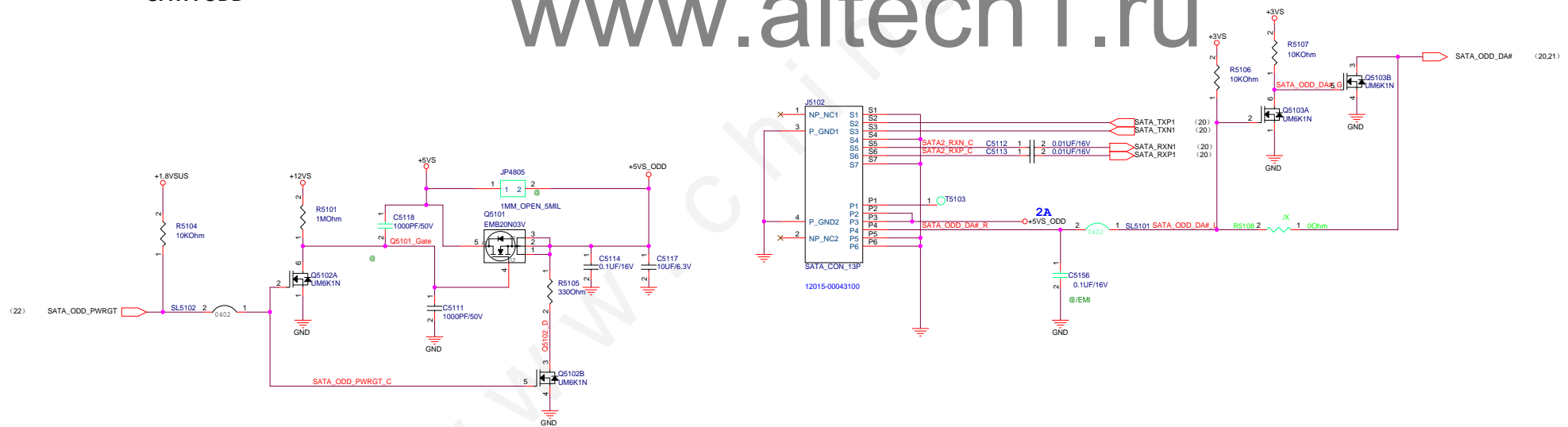
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

SATA HDD



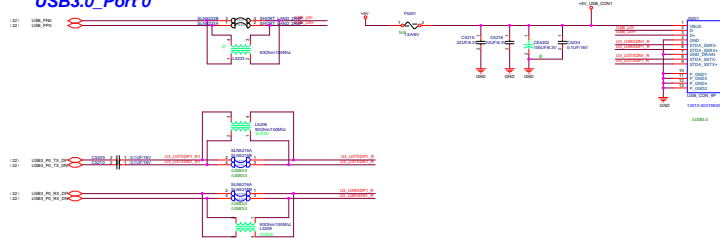
SATA ODD



X552MD

USB3.0_Port 0

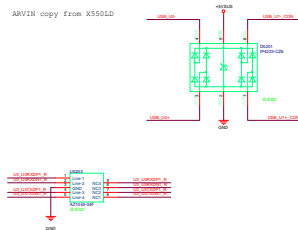
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X552MD

ESD-Protection

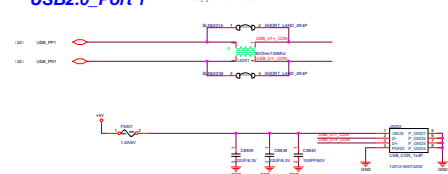
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X552MD

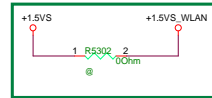
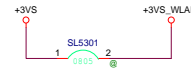
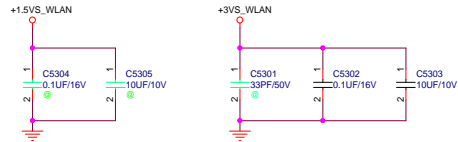
USB2.0_Port 1

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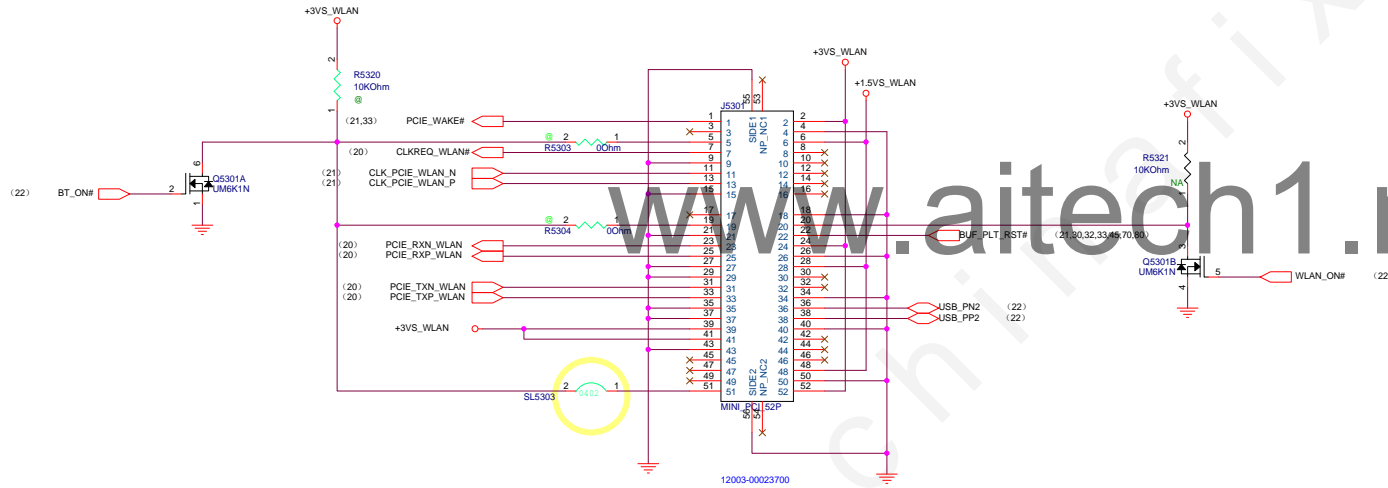


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0520-11 Dean Merge BOM L3000 L5301 L2603 L2604 L2707
=> 1200HM/2A 09G013120802



0309-11 Dean cost check keypart list
=> unstuff C5304, C5305




2nd source:
12003-00024000

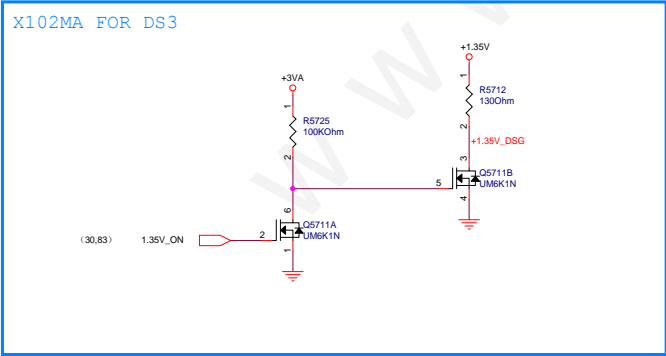
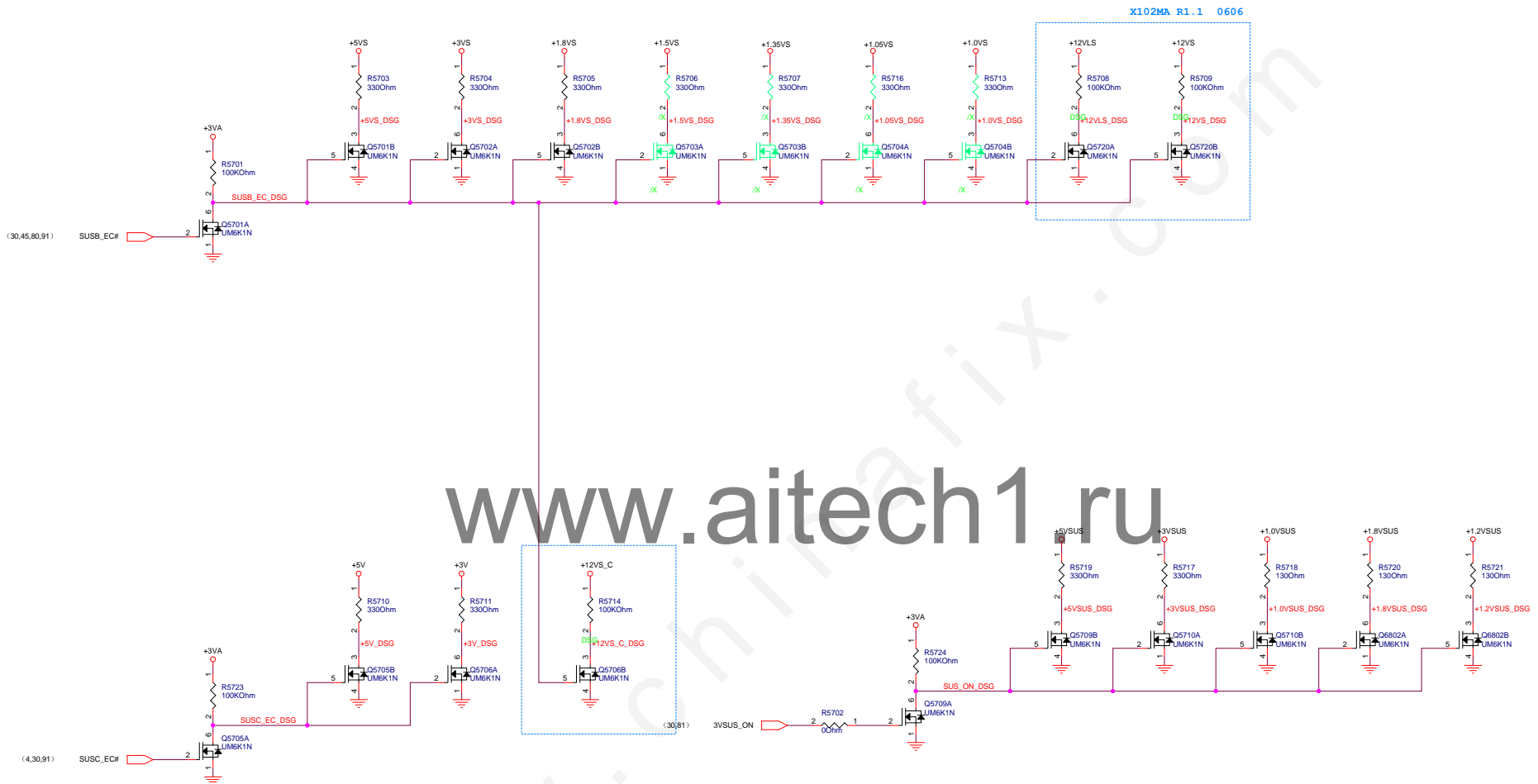
www.aitech1.ru

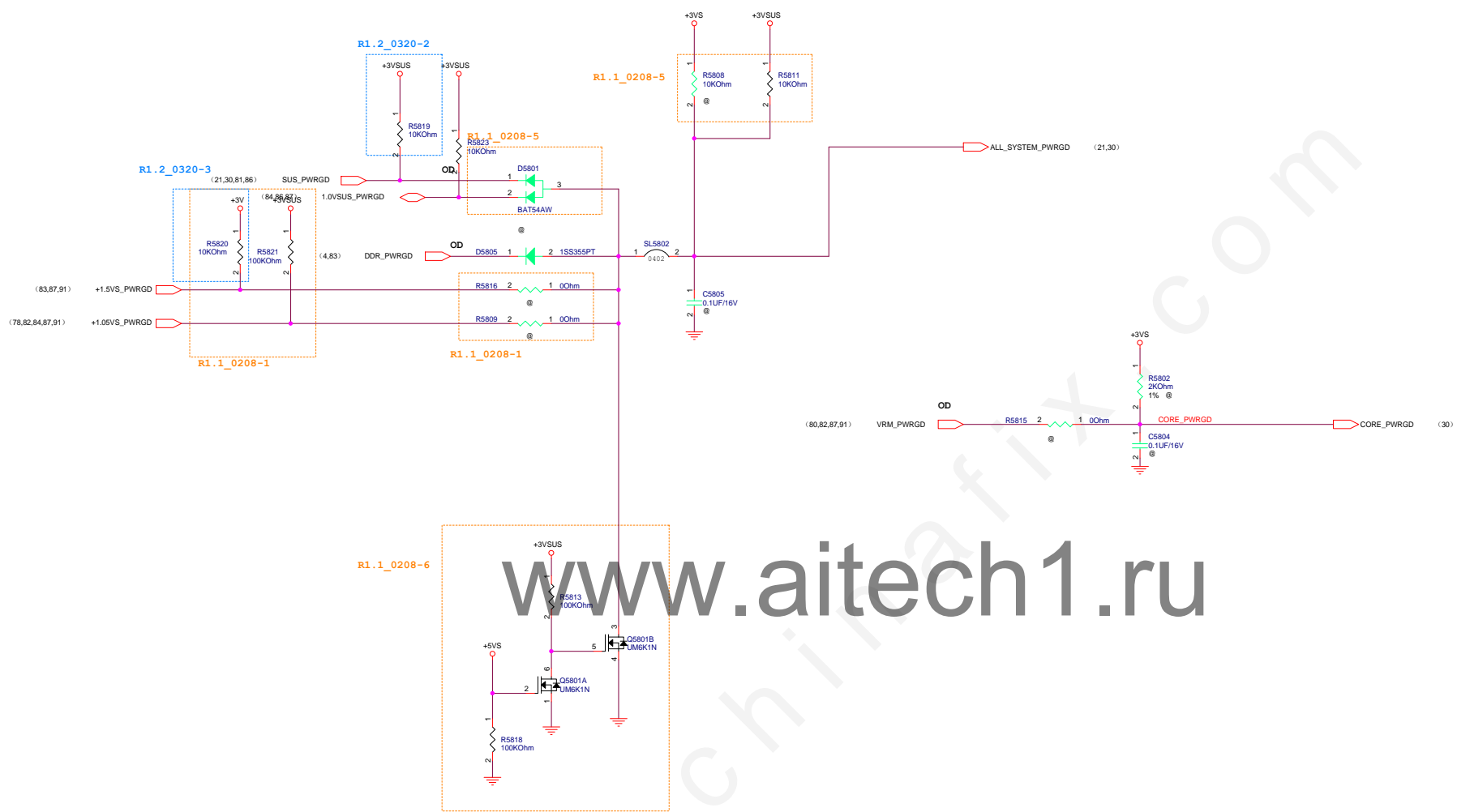
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ASUSTeK COMPUTER INC. NB8		Engineer: RD1_EE2-1	
Size A3	Project Name X102MA Bay Trail-M	Rev 1.0	
Date: Friday, March 14, 2014		Sheet	55 of 98

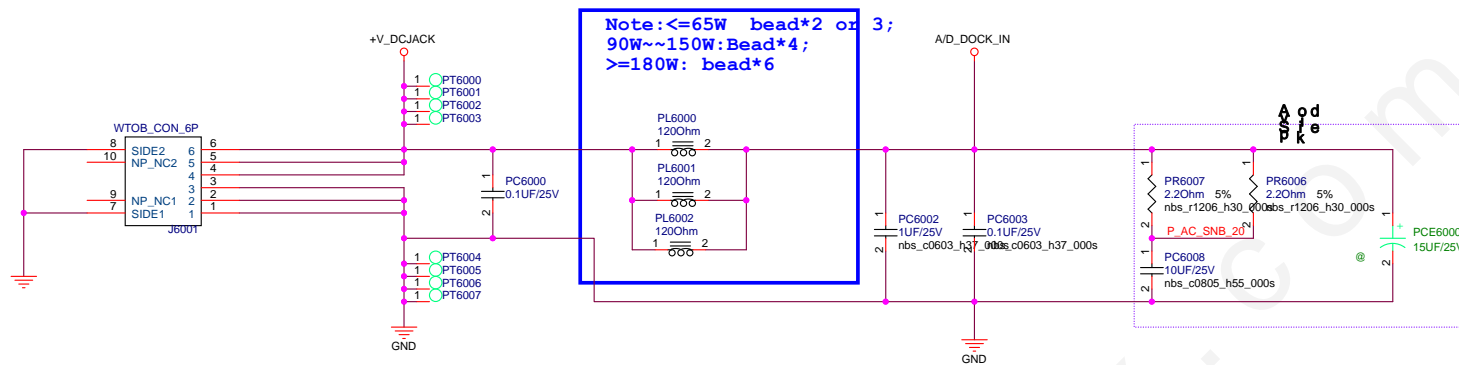
www.aitech1.ru





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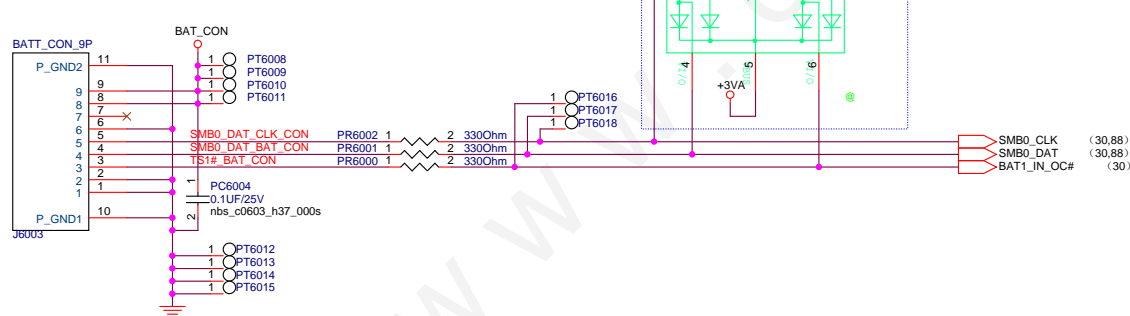
<Variant Name>			Title : ****	
			Engineer: SZ_SYS2	
Size	Project Name			Rev
C	X551CA			1.0
Date: Friday, March 14, 2014		Sheet 59 of 85		



Battery Connector

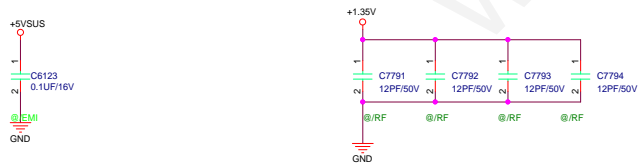
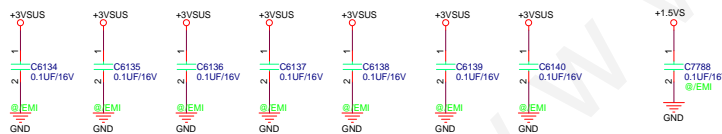
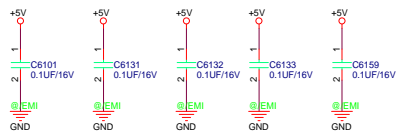
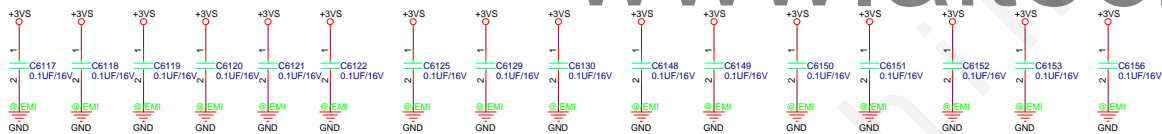
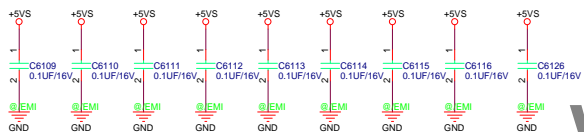
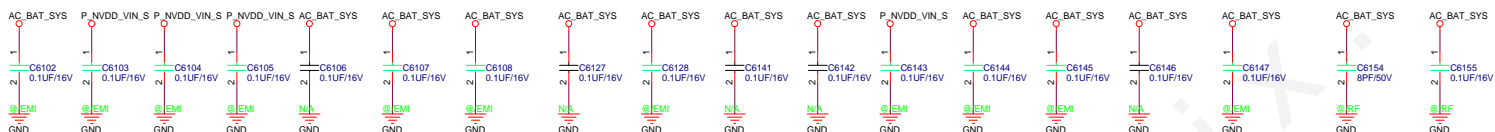
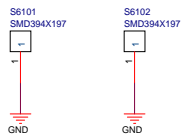
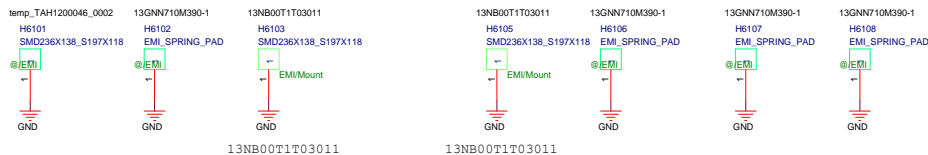
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BAT_CON 婉 pin3 婉 pin7 婉 NC, 婉 璜璜GND.



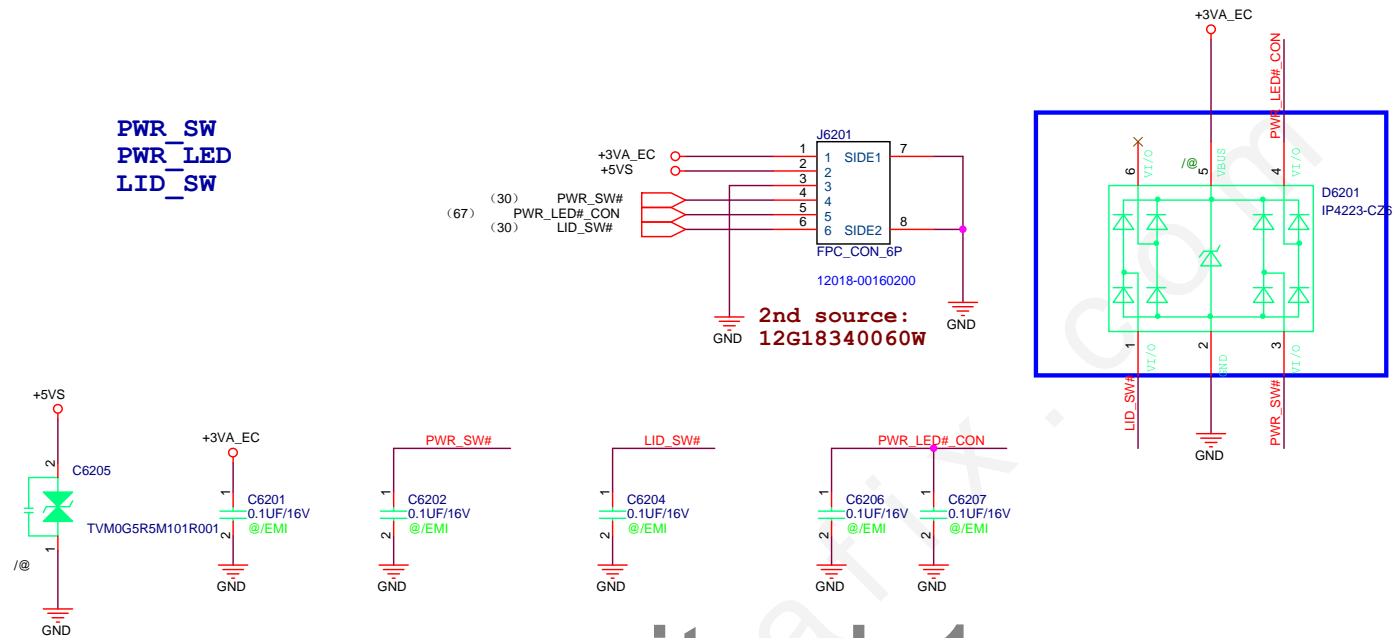
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ASUSTeK COMPUTER INC.		Engineer:	
Size	Project Name	Rev	
Custom	KX STD	R1.2	
Date: Friday, March 14, 2014		Sheet 60 of 98	



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<Variant Name>			
File			
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Size	Document Number		Rev
C	X590		1.0
Date:	Friday, March 14, 2014	Sheet	81 of 88



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<Variant Name>

ASUS		Title : B TO B CONNECTOR	
ASUSTeK COMPUTER INC.		Engineer: SZ2_Team3	
Size B	Project Name X550LC		Rev 1.0
Date: Friday, March 14, 2014		Sheet 62 of 98	

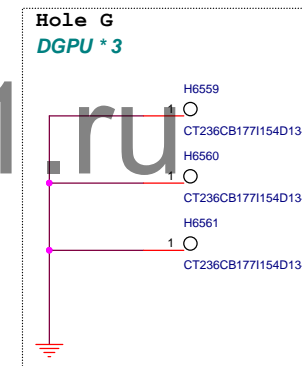
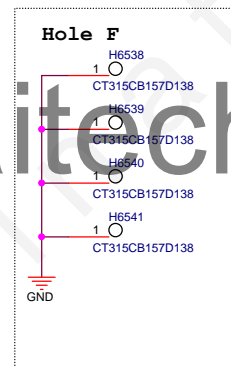
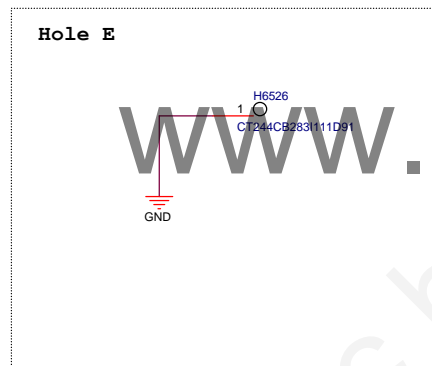
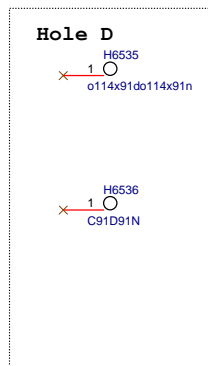
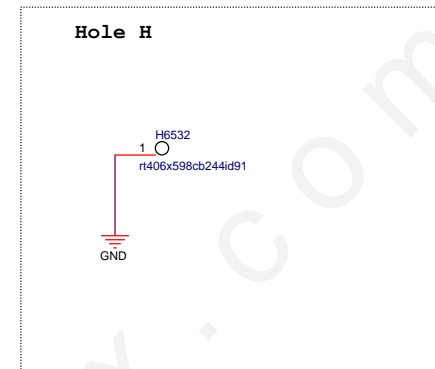
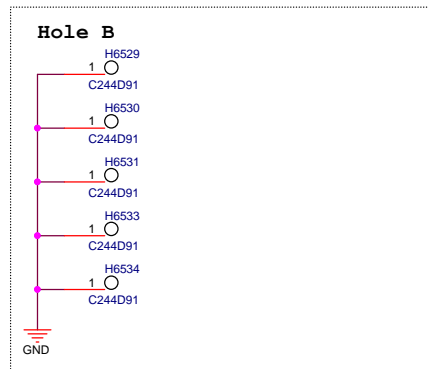
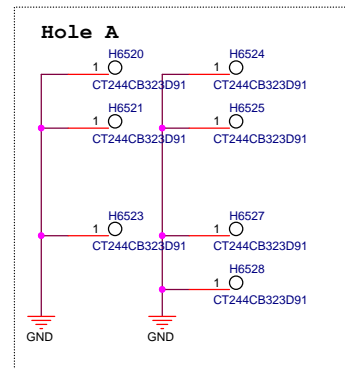
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UART Debug Board

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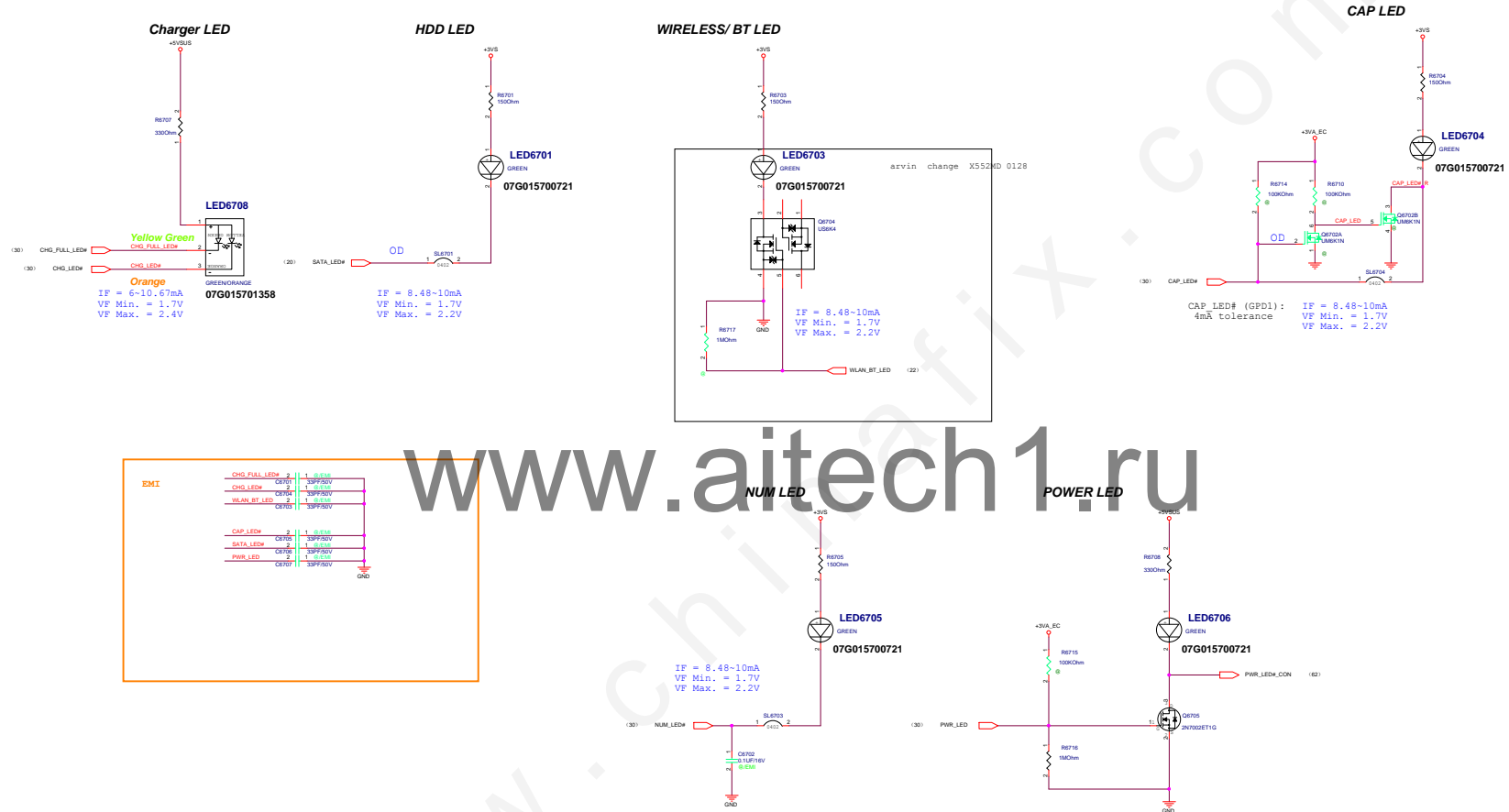
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ASUSTeK COMPUTER INC.		Engineer: RD1_EE2-1	
Size B	Project Name X102MA_Bay Trail-M		Rev 1.0
Date: Friday, March 14, 2014		Sheet 64	of 98

Screw Hole & SMT Nut

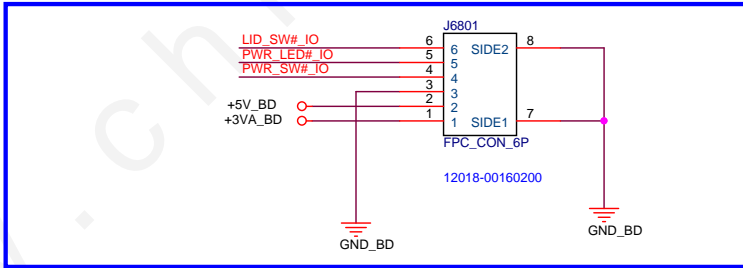
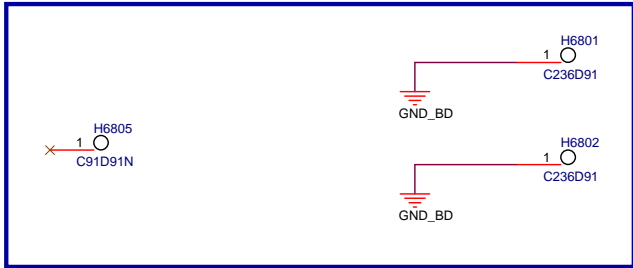
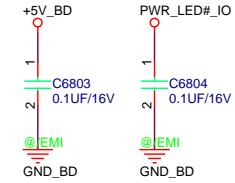
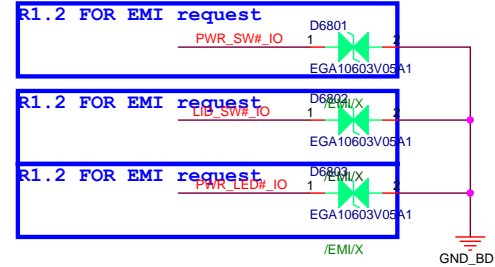
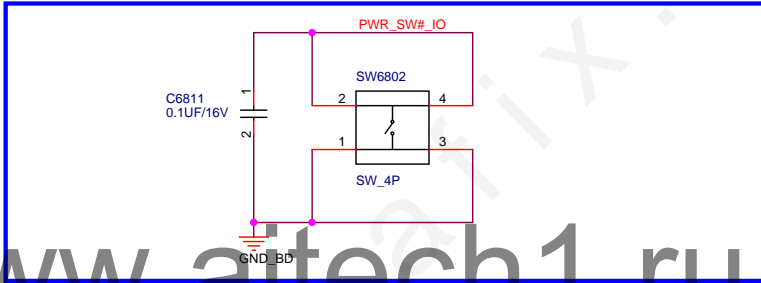
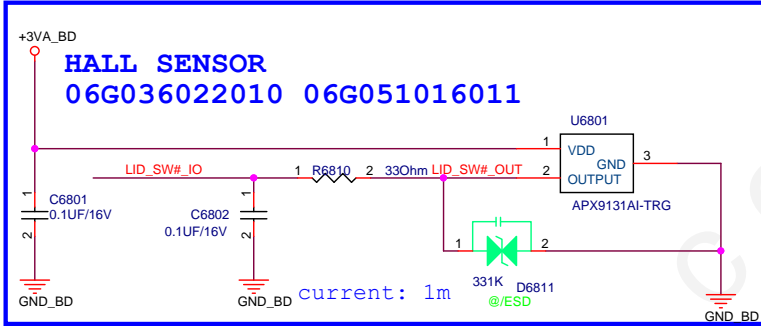
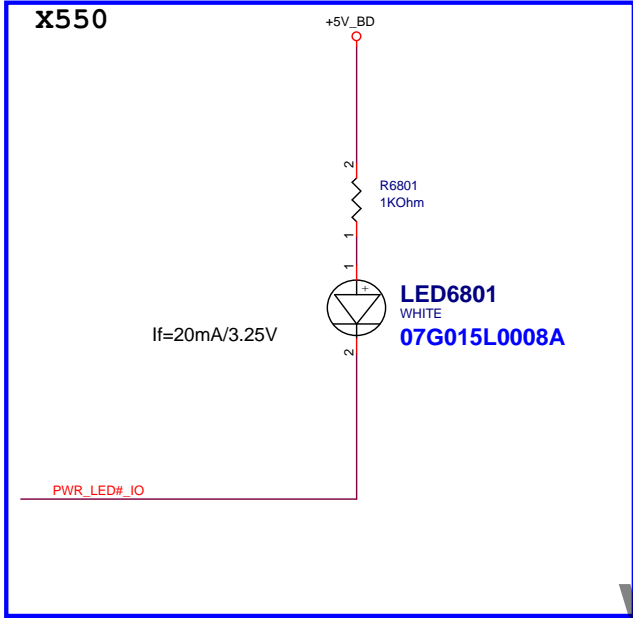


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LED indicator

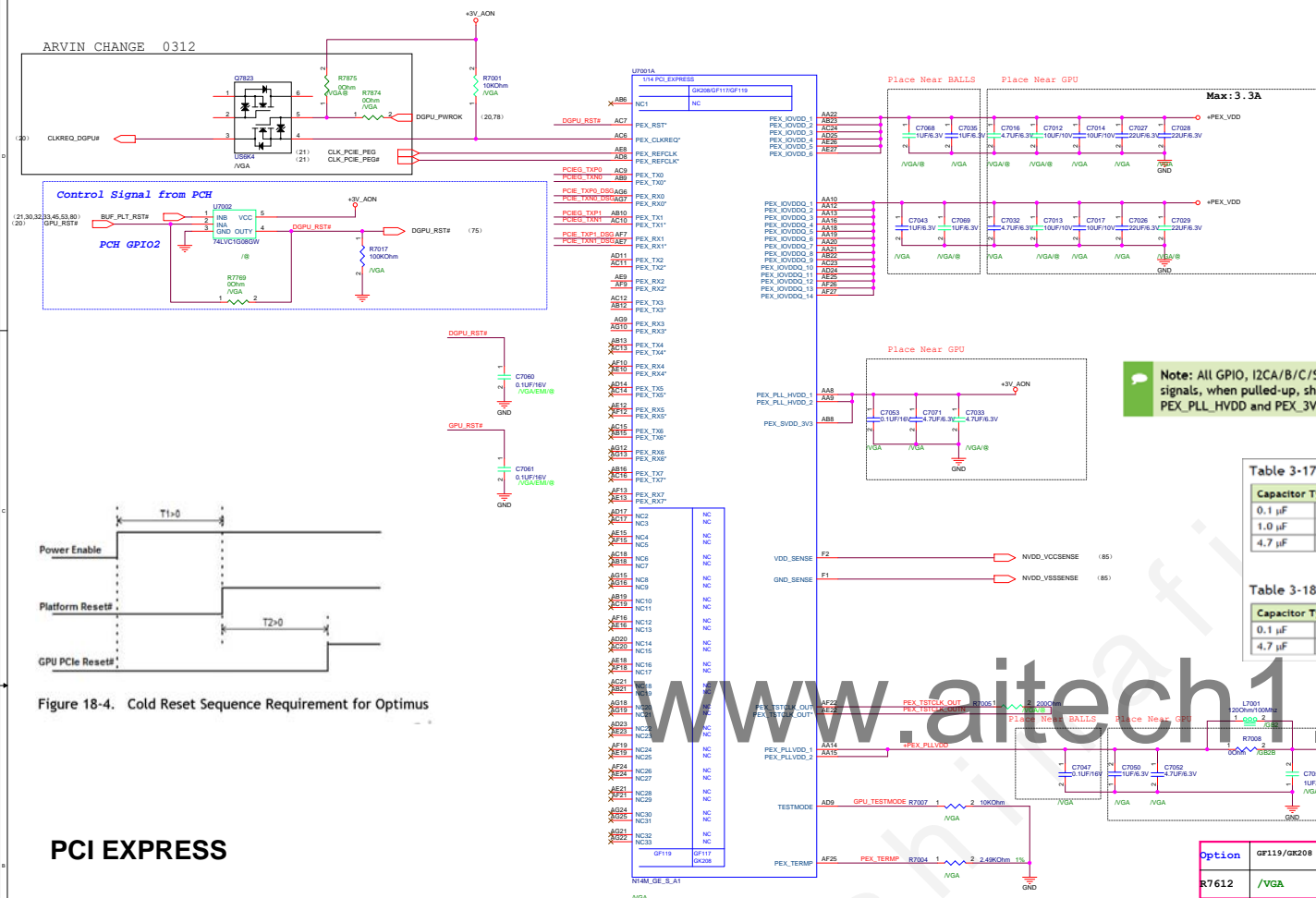


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		Title : EMI	
ASUSTeK COMPUTER INC.		Engineer: SZ_SYS2	
Size A	Project Name X551CA		Rev 1.0
Date: Friday, March 14, 2014		Sheet	69 of 98



Capacitor Type	Typical N14x Population	N15V-QM Population	N15S-GV Population	N15S-QM-GT Population	Location
1.0uF X6S 0402	4	4	4	1	Under GPU
4.7uF X6S 0603	2	2	2	1	Under GPU
10uF X5R 0805	4	4	4	1	Near GPU
22uF X5R 0805	4	4	4	1	Near GPU

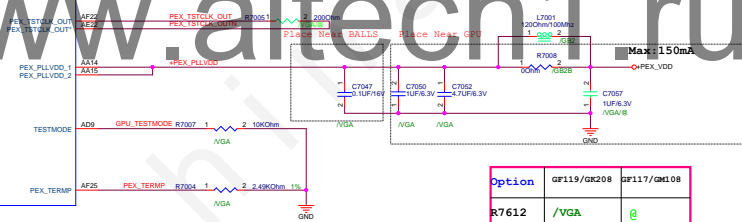
Note: All GPIO, I2CA/B/C/S, DAC_H/V_SYNC, PCIE Reset, CLKREQ#, XTAL, and JTAG signals, when pulled-up, should be connected to 3V3_AON power rail. Also PEX_PLL HVDD and PEX_3V3 SVDD must be sourced by 3V3_AON.

Table 3-17. PEX_PLLVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μ F	X6S	0402	1	Under GPU
1.0 μ F	X5R	0603	1	Near GPU
4.7 μ F	X5R	0805	1	Near GPU

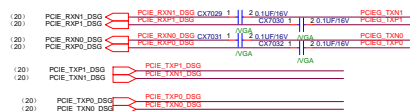
Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μ F	X5R	0402	1	Near GPU
4.7 μ F	X5R	0603	2	Near GPU

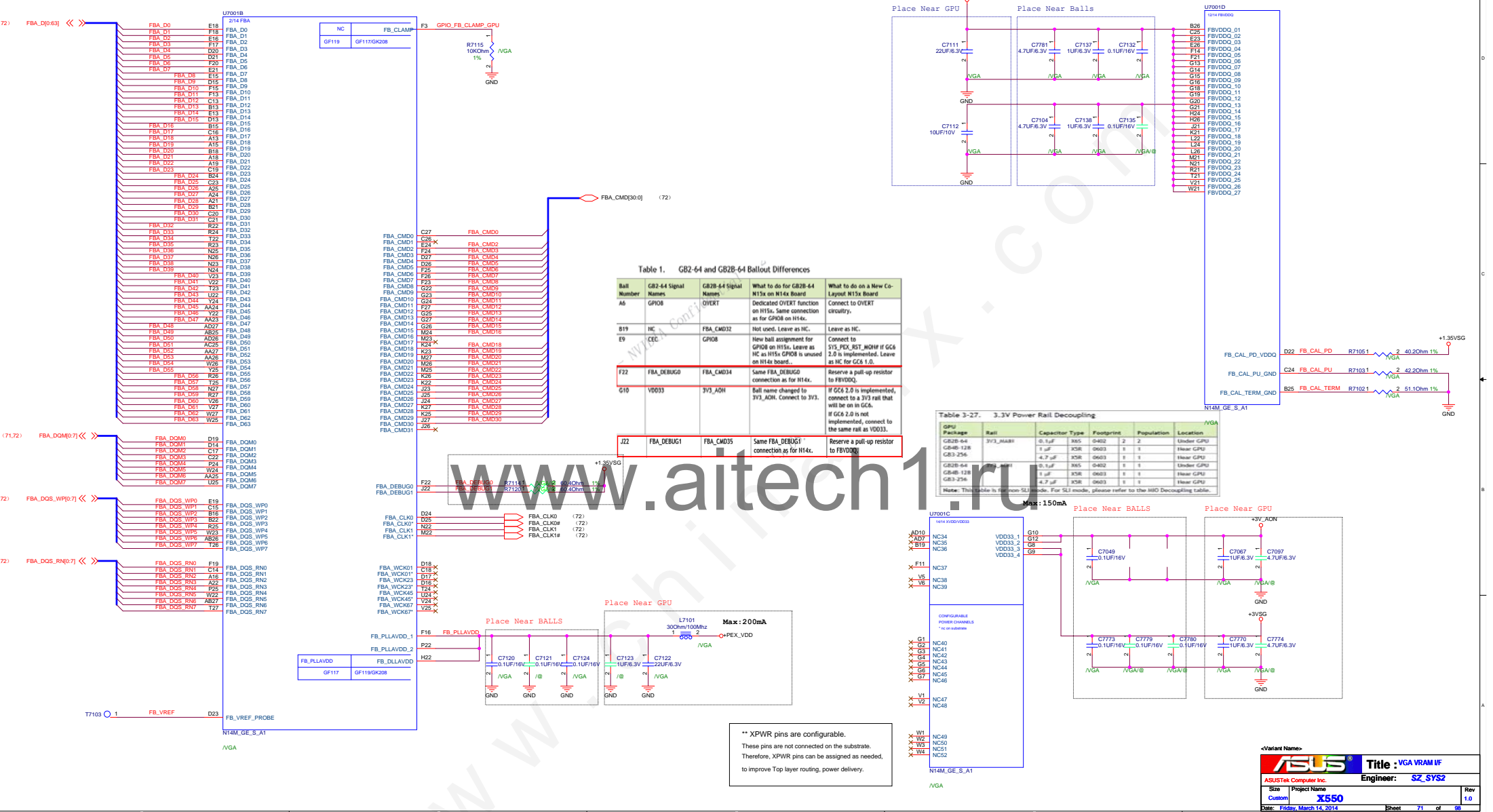


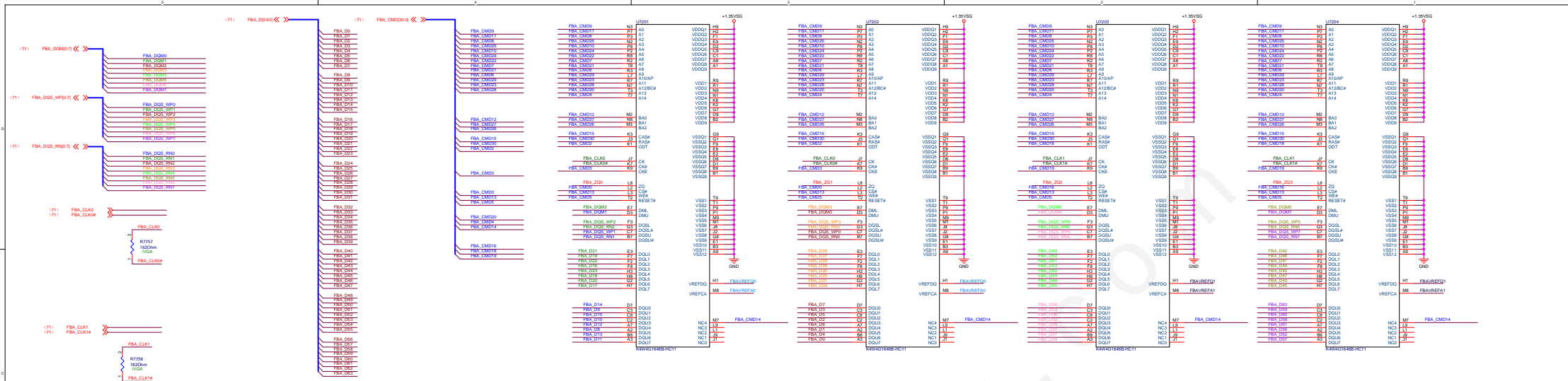
Option	GF119/GK208	GF117/GM10
R7612	/VGA	@

PCI EXPRESS

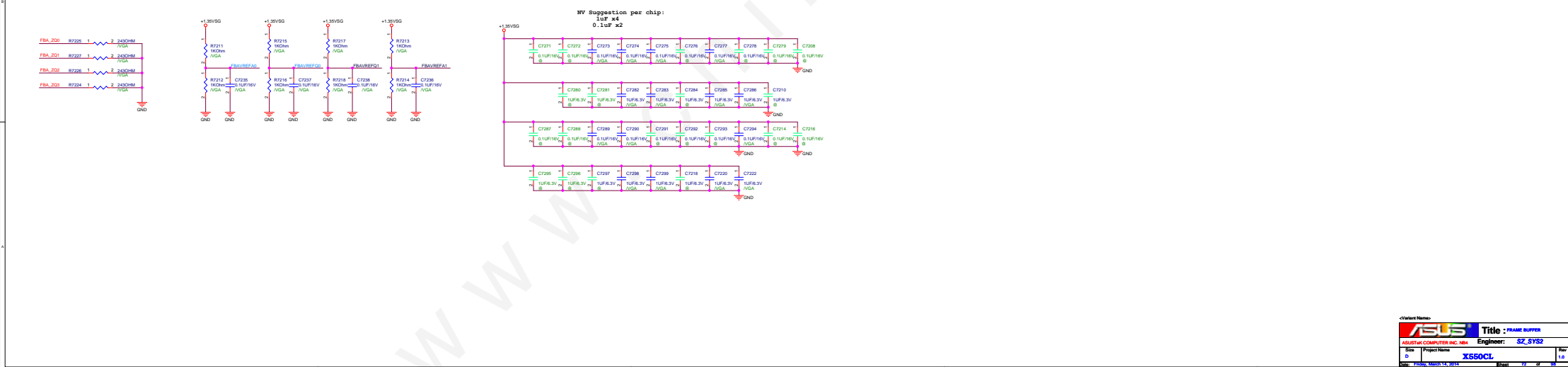


GPU MEMORY INTERFACE: PARTITION A



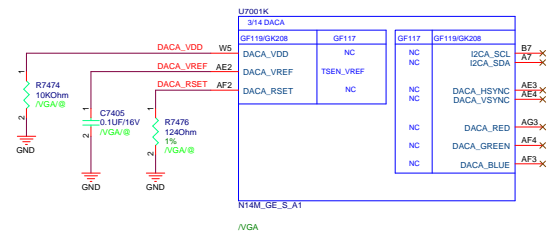


Memory_ID_Straps			
Vendor	DDR3L Memory Type	VRAM Vendor Part	Part Number
HYMIX	128M*16*4 PCS (1GB)	H57Q2G63DPR-11C (1800MHz)	03006-00040200
Micron	128M*16*4 PCS (1GB)	MT41J12M16JT-107G:K (1800MHz)	03006-00040500

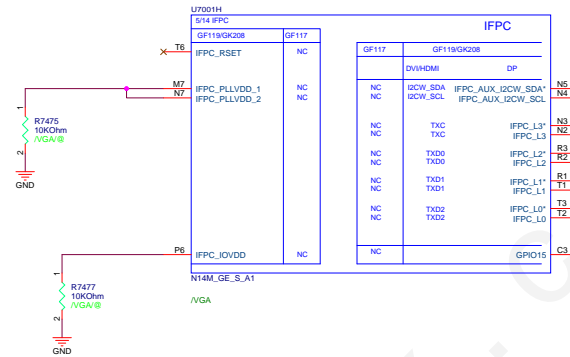


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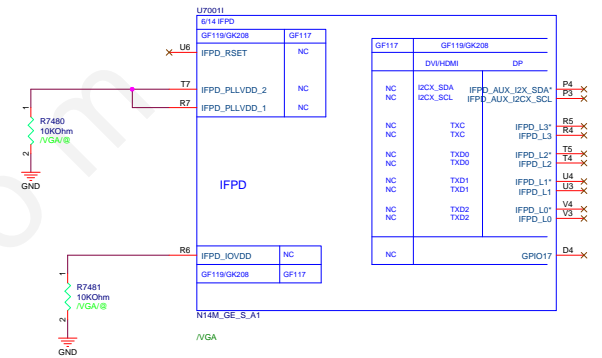
CRT DAC_A



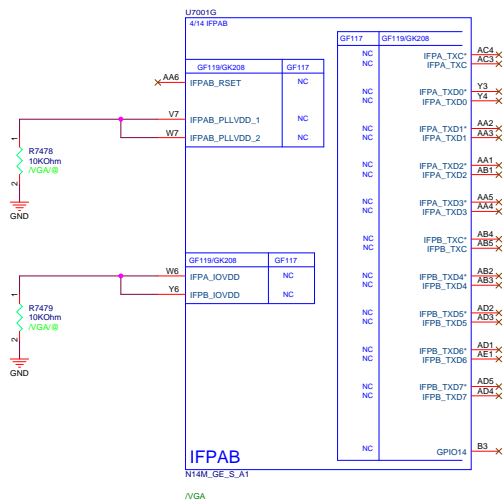
DP(link C)



DVI(link D)



LVDS IFPA/B



LVDS IFPE/F

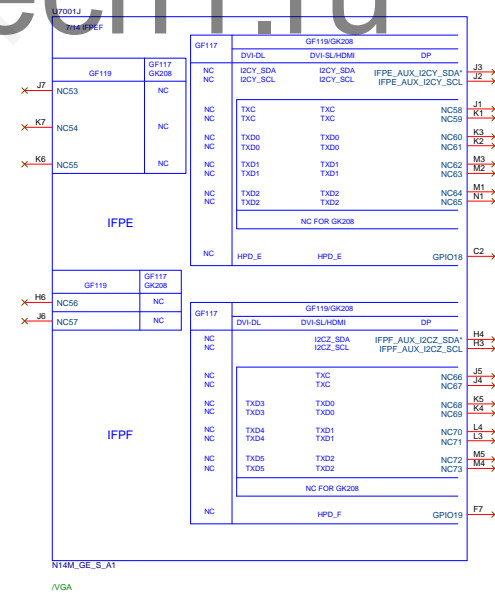
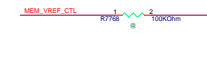
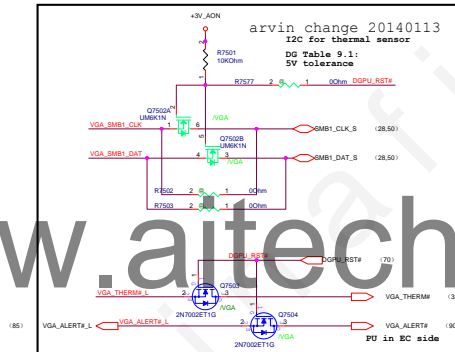


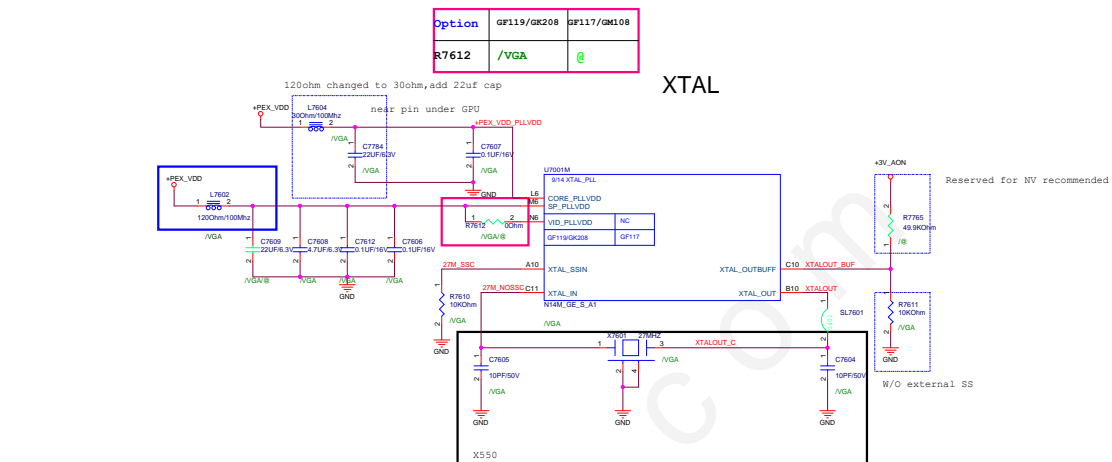
Table 114. GB2-64 and GB4-128 GPIO Description

Pin	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_A0H	I	FB Clamp Enable	
GPIO1	MEMO_VDDC1	I	Memory VDDC1	MEM_VDDC1 to boot FB150/12Q
GPIO2	LOCB_FB_P0H	O	Panel Backlight Pin Brightness Control	100 k pull-down
GPIO3	LOCB_VCC	O	Panel Power Enable	LOCB_VCC: 100k pull-down
GPIO4	LOCB_BLED1	O	Panel Backlight Enable	
GPIO5	Reserved			
GPIO6	FB_CLAMP_VGA_REQ	O	Active low FB Clamp toggle request	
GPIO7	Sink0H	O	Sink Low Latch Signal	100 k pull-down
GPIO8	OVERT	O	Active Low Thermal Catastrophic Over Temperature	100 k pull-up
GPIO9	ALERT	O	Active Low Thermal Alert	NbK pull-up
GPIO10	MEMO_VREF_CTL	O	Memory VREF Control	100 k pull-down
GPIO11	Phas_VDD	O	GPIO 100 VDD Phas Voltage	
GPIO12	PWR_LVL1	I	AC power detect or power adaptive input Phase Shedding	100 k pull-up
GPIO13	PDSI	I	Power Detect	10k pull-up to enable the pin (see Page 7)
GPIO14	HFD_A	I	Hot Plug Detect for HFD as displayPort or for IFFA when used as Hot Data D10	
GPIO15	HFD_C	I	Hot Plug Detect for HFD_C	See Page 73
GPIO16	FWD_LCK	O	JT Framer Lock signal	See Page 73
GPIO17	HFD_B	I	Hot Plug Detect for HFD_B	See Page 73
GPIO18	HFD_F	I	Hot Plug Detect for HFD_F	See Page 73
GPIO19	HFD_O or HFD_B	I	Hot Plug Detect for HFD or for IFFA used as displayPort	See Page 73
GPIO20	Reserved			
GPIO21	Reserved			

Table 7. GPIO Differences

GPIO Pin	CPU	Normal Function	Comments
GPIO8	HI5V-GA HI5S-GV	OVERT	Connect to OVERT circuitry.
	HI5S-GA/ GT	RESERVED in Hi4x systems or SYS_PXD_RST_M0M in Hi5x systems	The OVERT function is provided on the dedicated OVERT pin on GB2-64, which is on the same pin as GPIO8 on GB2-64. GPIO8 on GB2-64 is a system PEX reset monitor function for GC6 2.0. If HI5S-GA/GT are designed into Hi4x motherboard with GC6 1.0, leave GPIO8 as NC. If HI5S-GA/GT are designed into Hi5x motherboard with GC6 2.0, use GPIO8 as the SYS_PXD_RST_M0M function.
GPIO15, GPIO16, GPIO17, GPIO18, GPIO19	HI5V-GA HI5S-GV HI5S-GA/ GT	N/A Display HPD	Leave as NC Leave as NC if HPD function is not required. See Hi5x Design Guide, DG-06802-001, for which HPD link should be paired with which GPIO pin for its HPD function.
GPIO16	HI5V-GA	N/A	Leave as NC
	HI5S-GV HI5S-GA/ GT	RESERVED	Leave as NC
GPIO20	HI5V-GA	N/A	Leave as NC
	HI5S-GV HI5S-GA/ GT	RESERVED	Leave as NC
GPIO21	HI5V-GA HI5S-GV	N/A	Leave as NC Leave as NC
	HI5S-GA/ GT	RESERVED in Hi4x systems or GPU_PXD_RST_H0M in Hi5x systems	If HI5S-GA/GT are designed into Hi4x systems with GC6 1.0, leave GPIO21 as NC. If HI5S-GA/GT are designed into Hi5x motherboard with GC6 2.0, use GPIO21 as the GPU_PXD_RST_H0M function.

[illegible]



Need to check

USER[R32]
 STRAP0
 3GIO_PAD_CFG[3:0]
 STRAP1
 PCI_DEVID[3:0]
 STRAP2

+3V_AGN

R7611 4.9kOhm
 R7604 12kOhm
 R7627 30kOhm
 R7626 15kOhm
 R7607 68kOhm
 R7628 10kOhm
 R7625 10kOhm
 R7606 10kOhm
 R7624 10kOhm
 R7623 512Ohm
 R7622 512Ohm

+3VSG

RAM_CFG[3:0]
 XCLK27_TV_MODE[2:0]
 SUB_VENDOR_SLOT_CLK_CFG_PEX_PLL_EN_TERM100

R7616 4.9kOhm
 R7617 15kOhm
 R7618 10kOhm
 R7619 10kOhm
 R7620 15kOhm
 R7621 10kOhm
 R7624 10kOhm
 R7623 512Ohm
 R7622 512Ohm

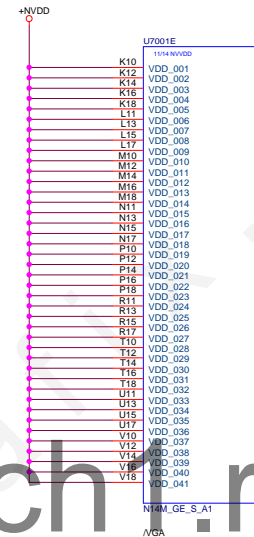
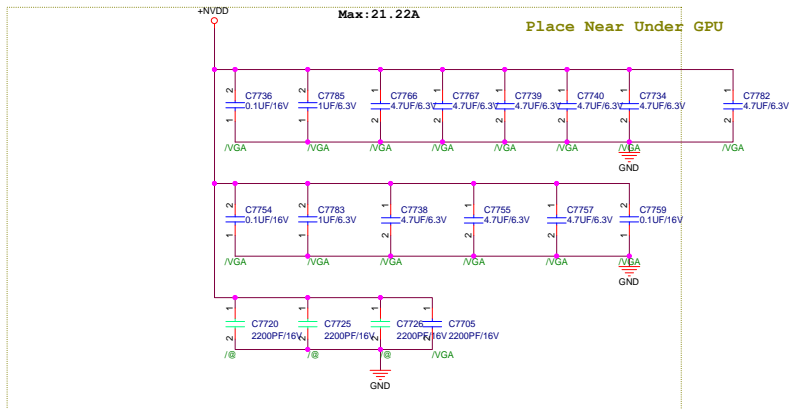
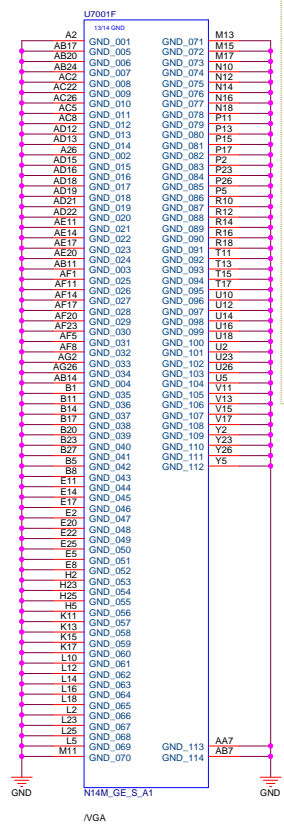
512x8: change R7618 to 24.9kOhm(10021249214010)

[illegible]

GPU Model / GPU		GPU Size	GPU	VRAM Vendor	Type	FVDD / FVDDQ	Config	VRAM P/N	Max Speed CLK	I/O (M/s)	RAM CFG	ROM Size	Status									
GM108	N155-GT/GM	Hynix	DDR3	1.5V/1.5V	128Mb*6	H5TC2G63F-1R-11C	900MHz	NA	0x6	PD 35K	Preliminary											
													Micron	DDR3	1.5V/1.5V	128Mb*6	MT41J28M16T-093G-K	1000MHz	1322	0x7	PD 45K	Preliminary
		Hynix	DDR3	1.5V/1.5V	256Mb*6	H5TC4G63AF-1R-11C	1000MHz	NA	0x0	PD 5K	Preliminary											
												Micron	DDR3	1.5V/1.5V	256Mb*6	MT41J256M16HA-093G-E	1000MHz	1322	0x1	PD 10K	Preliminary	
																						Samsung
		Hynix	DDR3L	1.35V/ 1.35V	128Mb*6	H5TC2G63F-1R-11C	900MHz	NA	0x9	PU 10K	Preliminary											
												Micron	DDR3L	1.35V/ 1.35V	128Mb*6	MT41J28M16T-093G-K	900MHz	1322	0xA	PU 15K	Preliminary	
																						Samsung
		Hynix	DDR3L	1.35V/ 1.35V	256Mb*6	H5TC4G63AF-1R-11C	900MHz	NA	0xC	PD 20K	Preliminary											
												Micron	DDR3L	1.35V/ 1.35V	256Mb*6	MT41J256M16HA-093G-E	900MHz	1322	0x4	PD 25K	Preliminary	
																						Samsung
	Note: Extended Rank (up to 8) with Single Rank Reported																					
	N155-GT/GM	Hynix	DDR3	1.5V/1.5V	256Mb*6	H5TC4G63AF-1R-11C	1000MHz	NA	0x0	PD 5K	Preliminary											
													Micron	DDR3	1.5V/1.5V	256Mb*6	MT41J256M16HA-093G-E	1000MHz	1322	0x0	PD 10K	Preliminary
		Hynix	DDR3L	1.35V/ 1.35V	256Mb*6	H5TC4G63AF-1R-11C	900MHz	NA	0xC	PD 20K	Preliminary											
												Micron	DDR3L	1.35V/ 1.35V	256Mb*6	MT41J256M16HA-093G-E	900MHz	1322	0x4	PD 25K	Preliminary	
																						Samsung

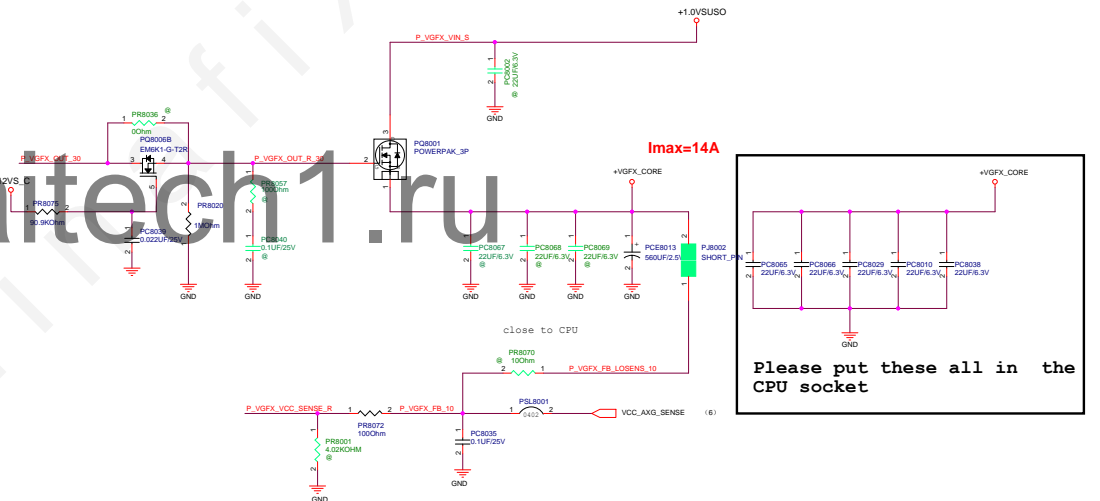
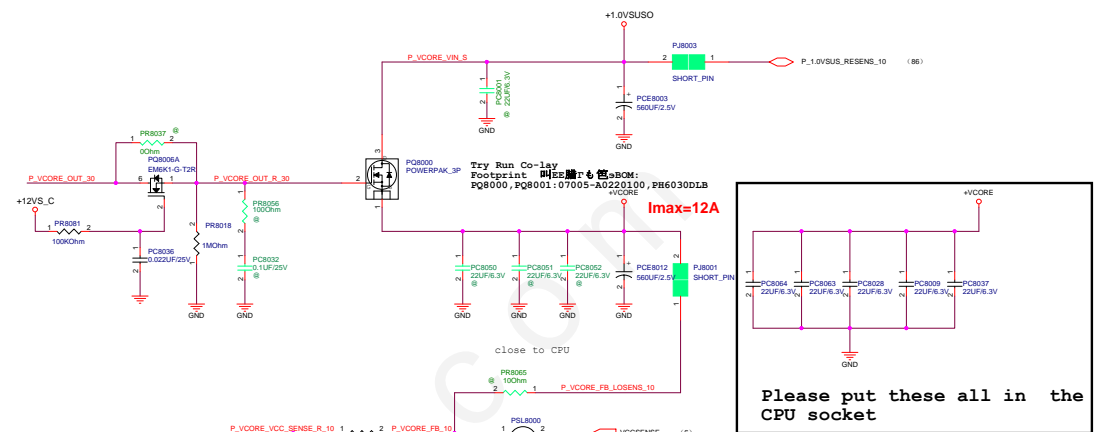
NVVDD GROUND

NVVDD POWER AND DECOUPLING

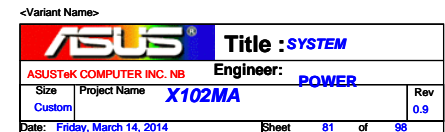


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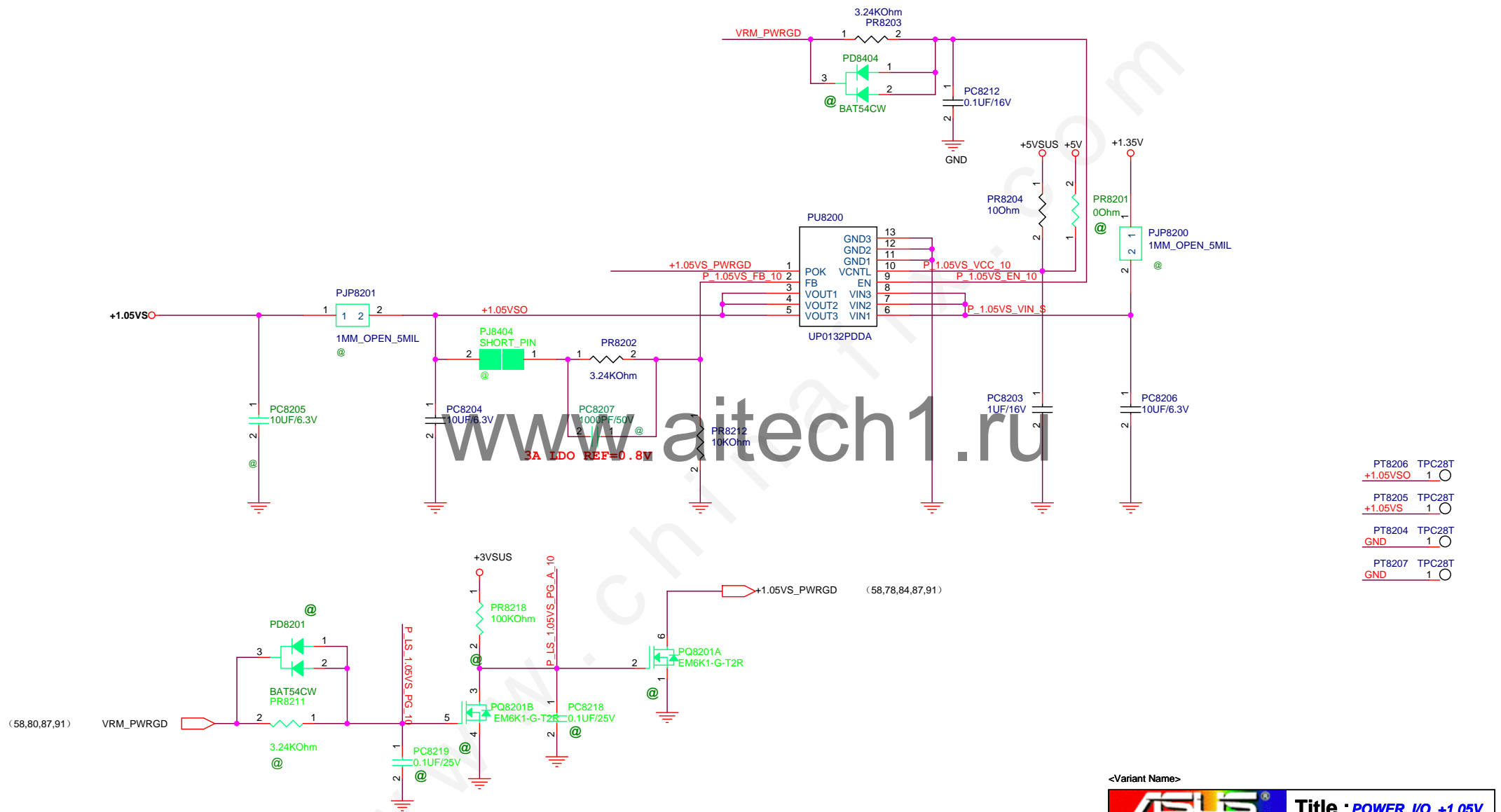
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SUS_PWRGD SUS_PWRGD (21,30,58,86)

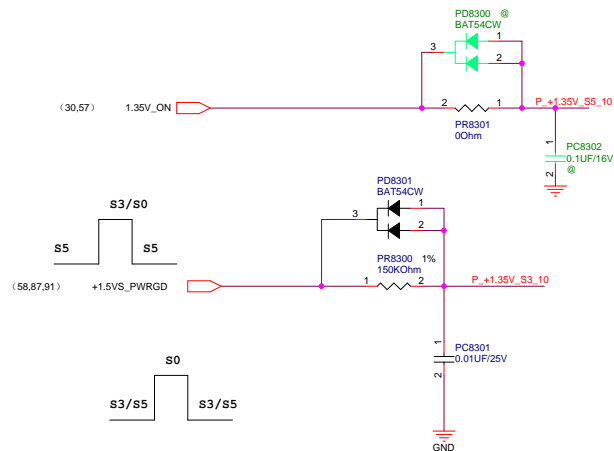


+1.05VS POWER SUPPLY



<Variant Name>

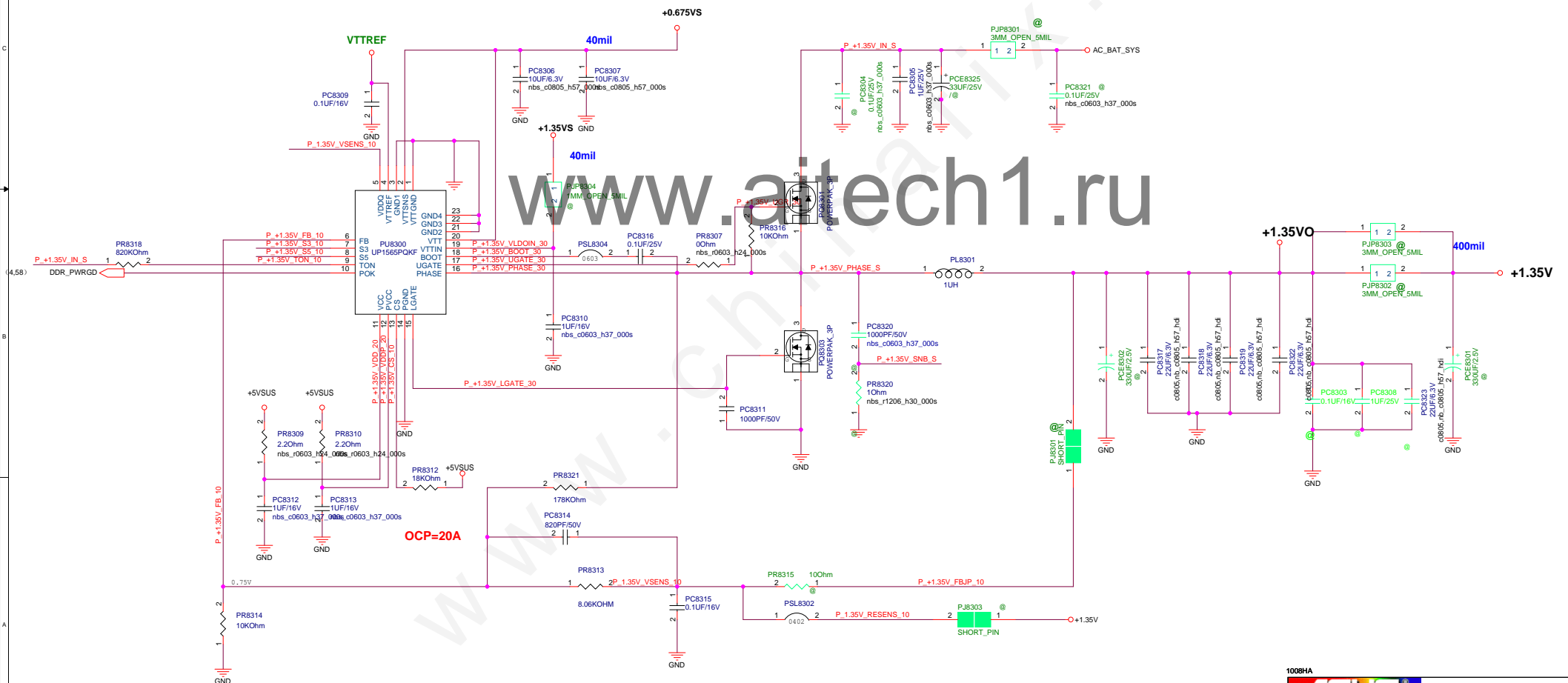
ASUS		Title : POWER_I/O_+1.05V	
ASUSTeK COMPUTER INC.		Engineer: Jeff Kao	
Size	Project Name	X102MA Bay Trail-M	Rev 1.0
Custom			
Date: Friday, March 14, 2014		Sheet 82	of 98



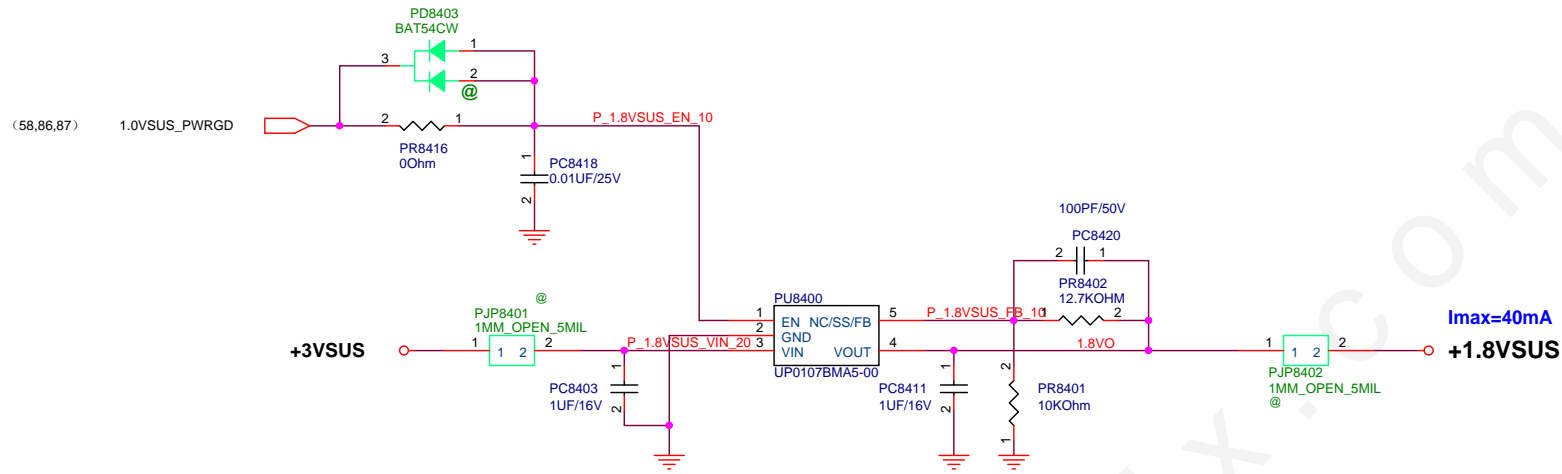
S3 And S5 Truth Table

State	S3	S5	VDDQ
S0	Hi	Hi	On
S3	Low	Hi	On
S4/S5	Low	Low	Off (Discharge)

State	VTTREF	VTT
S0	On	On
S3	On	Off(Hi-Z)
S4/S5	Off (Discharge)	Off (Discharge)



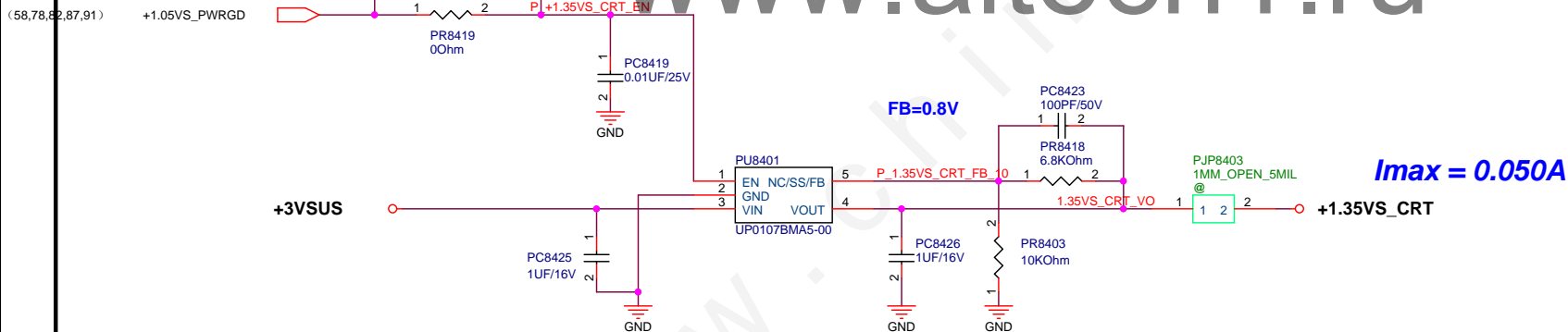
+1.8VSUS POWER SUPPLY



PT8406	TPC28T
+1.8VSUS	1
PT8404	TPC28T
GND	1
PT8405	TPC28T
GND	1

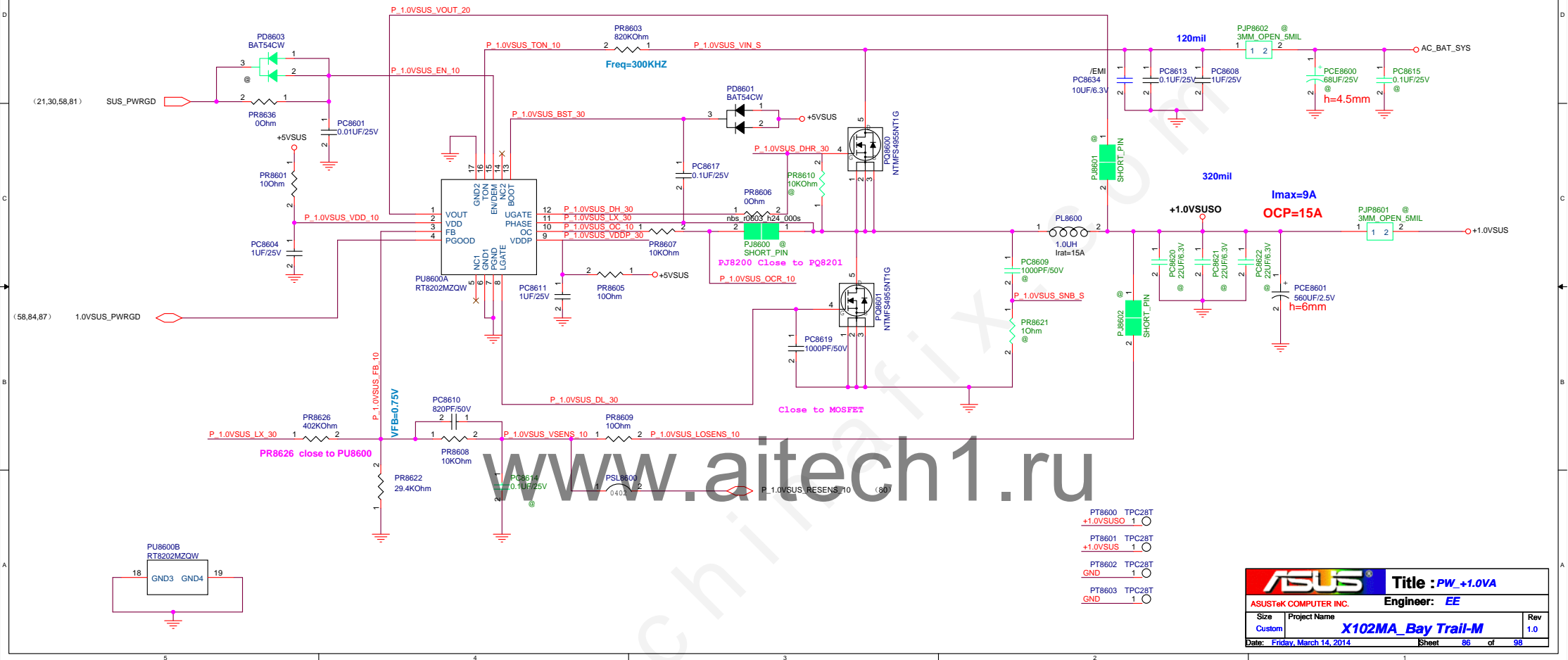
10.8

+1.35VS_CRT

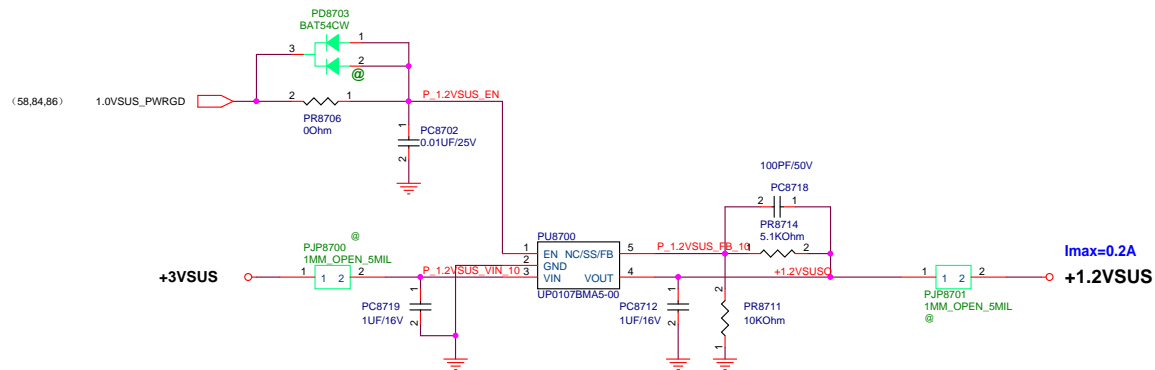


ASUS		Title : PW_+1.8VA	
ASUSTeK COMPUTER INC.		Engineer:	
Size	Project Name	X200MA_Bay Trail-M	Rev 1.0
Custom			
Date: Friday, March 14, 2014		Sheet	84 of 98

+1.0VSUS POWER SUPPLY

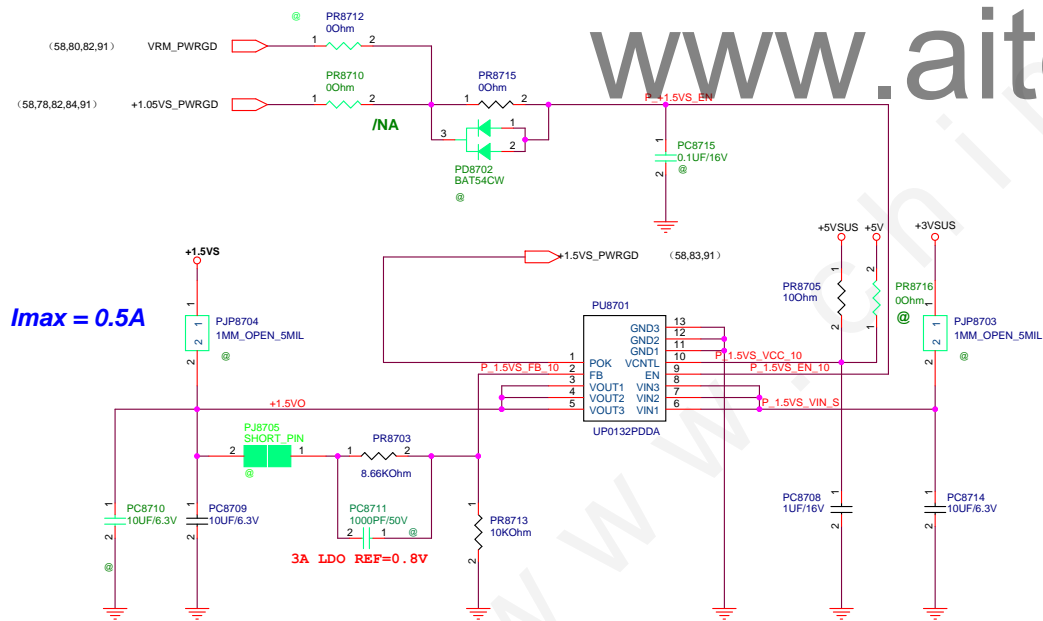


+1.2VSUS & +1.5VS POWER SUPPLY



PT8706 TPC28T
+1.2VSUSO 1
PT8705 TPC28T
+1.2VSUS 1
PT8704 TPC28T
GND 1
PT8707 TPC28T
GND 1

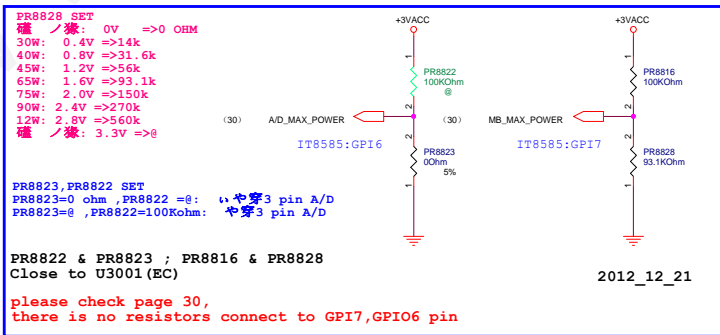
+1.5VS



PT8710 TPC28T
+1.5VO 1
PT8709 TPC28T
+1.5VS 1
PT8708 TPC28T
GND 1
PT8711 TPC28T
GND 1

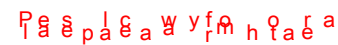
<Variant Name>

ASUS		Title : PW_1.2VA&1.5VS	
ASUSTeK COMPUTER INC.		Engineer: EE	
Size	Project Name	Rev	
Custom	X102MA Bay Trail-M	1.0	
Date: Friday, March 14, 2014		Sheet	87 of 98



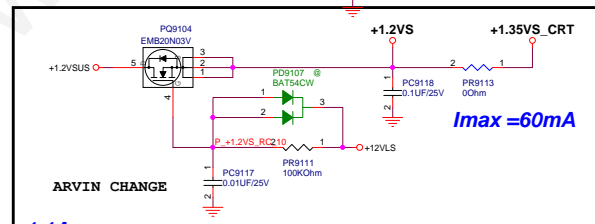
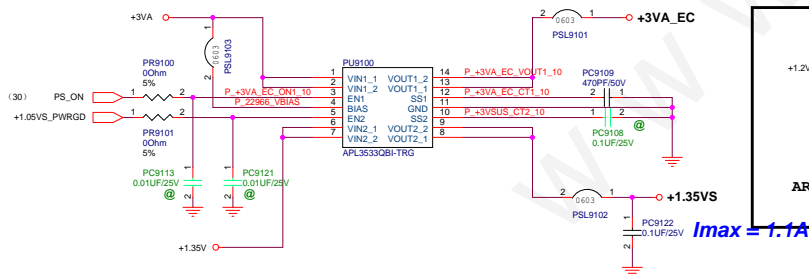
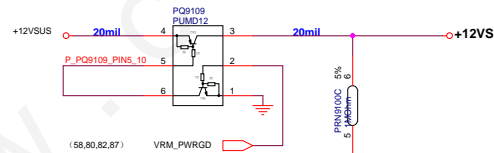
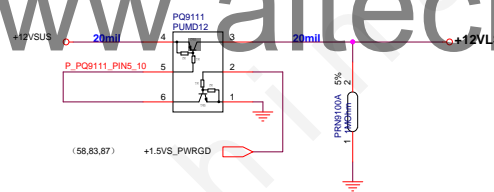
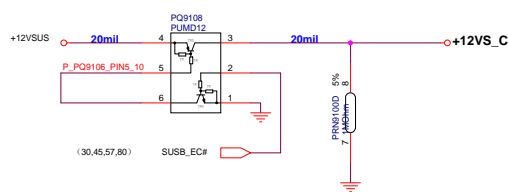
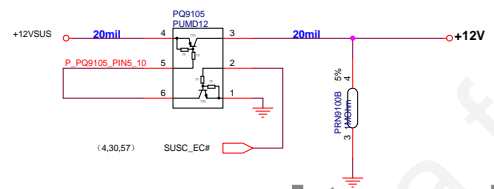
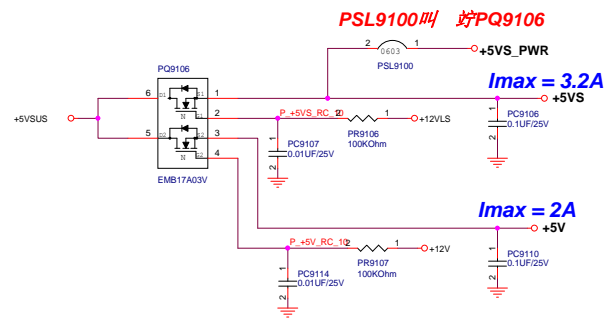
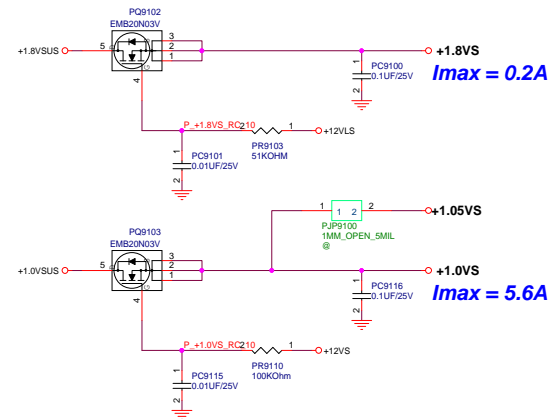
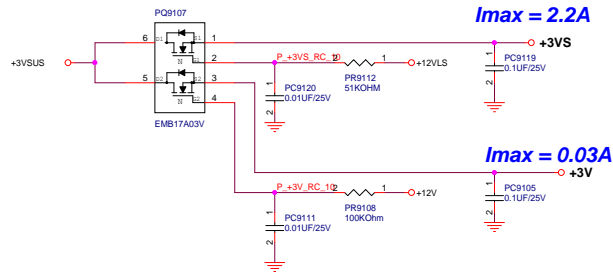
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<Variant Name>		
		Title : POWER_+VGFX_CORE
ASUSTeK COMPUTER INC.		Engineer: RD1_EE3
Size	Project Name	Rev
Custom	S200T_Bay Trail-M	1.0
Date: Friday, March 14, 2014		Sheet 09 of 09



dGPU GPIO9 pull low, GPU down to 1/4 frequency
dGPU GPIO12 pull low, GPU down to P8

Load Switch



<Variant Name>

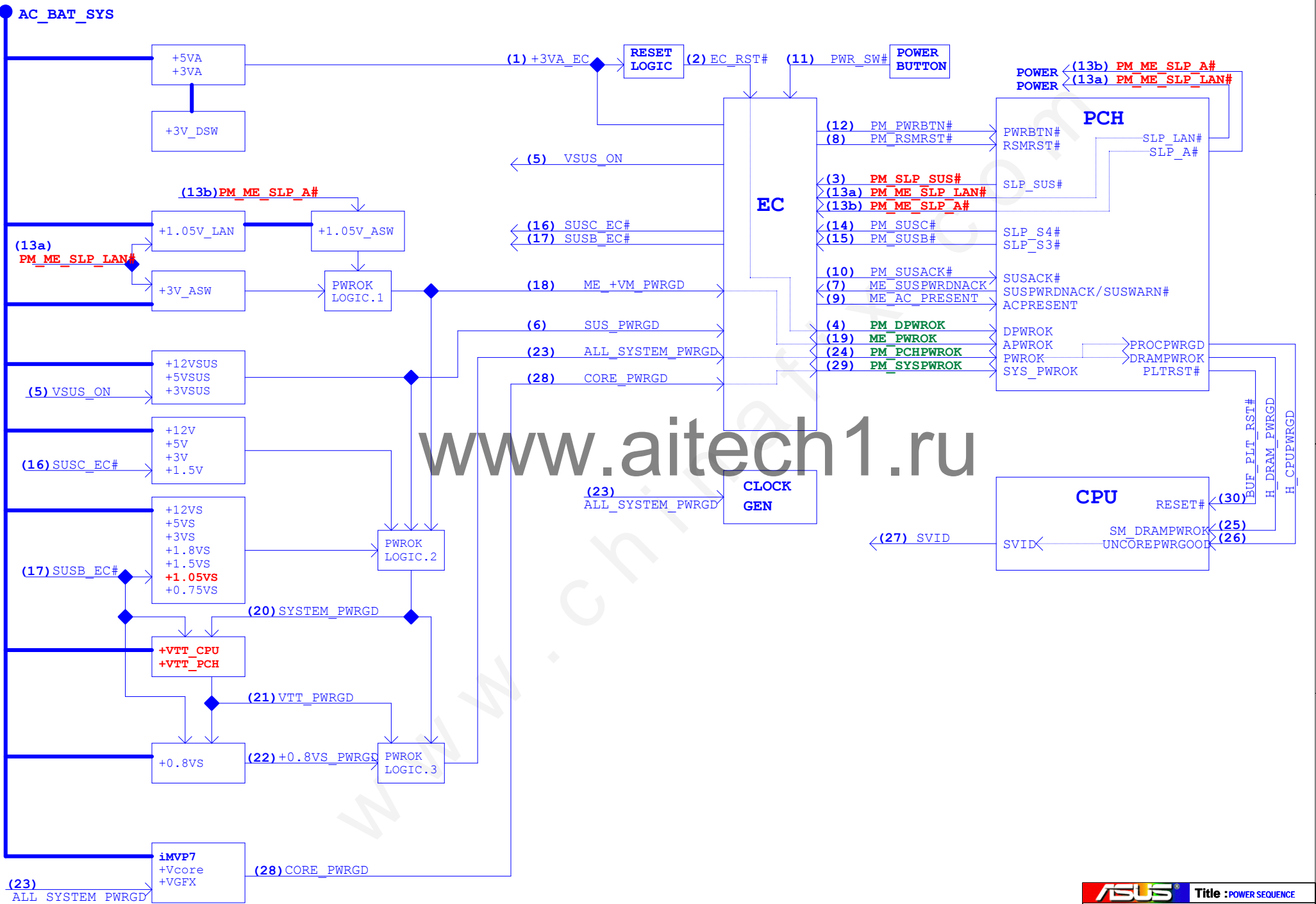
ASUS		Title : Load Switch	
ASUSTeK COMPUTER INC. NB		Engineer:	
Site	Project Name	Rev	
Custom	X102MA Bay Trail-M	1.0	
Date: Friday, March 14, 2014	Sheet	51	of 98



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[illegible]



AC-IN Mode

- 1 +3VA/+5VA/+3VA_EC
- 2 EC_RST#
- VccDSW
- 3 PM_SLP_SUS#
- 4 PM_DPWROK
- 5 VSUS_ON
- +3VSUS/+5VSUS
- SUS_PWRGD
- 7 ME_SusPwrDnAck
- 8 PM_RSMRST#
- 9 ME_AC_PRESENT
- 10 PM_SUSACK#
- 11 PWR_SW#
- 12 PM_PWRBTN#
- 13(a) PM_ME_SLP_LAN#
- 13(b) PM_ME_SLP_A#
- 14 PM_SUSC#
- 15 PM_SUSB#
- +105VM_LAN
- +1.05VM/+3VM
- 16 SUSC_EC#
- +1.5V/+3V/+5V
- 17 SUSB_EC#
- +0.75VS/+1.5VS//+1.8VS/+3VS/+5VS
- 18 ME_+VM_PWRGD
- 19 ME_PWROK
- 20 SYSTEM_PWRGD
- +VTT_CPU
- 21 +VTT_CPU_PWRGD
- +0.8VS
- 22 +0.8VS_PWRGD
- 23 ALL_SYSTEM_PWRGD
- 24 PM_PCHPWROK
- 25 H_DRAM_PWRGD
- 26 H_CPUPWRGD
- 27 SVID
- +VCORE
- +VccGFX
- 28 VRM_PWRGD
- 29 PM_SYSPWROK
- 30 BUF_PLT_RST#



U53 Power-On Sequence
Timing Diagram Rev.0.14

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U53 Power-On Sequence
Timing Diagram Rev.0.14

- 1 +3VA/+5VA/+3VA_EC
- 2 EC_RST#
- VccDSW
- 3 PM_SLP_SUS#
- 4 PM_DPWROK
- 5 PWR_SW#
- 6 VSUS_ON
- +3VSUS/+5VSUS
- 7 SUS_PWRGD
- 8 ME_SusPwrDnAck
- 9 PM_RSMRST#
- 10 ME_AC_PRESENT
- 11 PM_SUSACK#
- 12 PM_PWRBTN#
- 13(a) PM_ME_SLP_LAN#
- 13(b) PM_ME_SLP_A#
- 14 PM_SUSC#
- 15 PM_SUSB#
- +105VM_LAN
- +1.05VM/+3VM
- 16 SUSC_EC#
- +1.5V/+3V/+5V
- 17 SUSB_EC#
- +0.75VS/+1.5VS//+1.8VS/+3VS/+5VS
- 18 ME_+VM_PWRGD
- 19 ME_PWROK
- 20 SYSTEM_PWRGD
- +VTT_CPU
- 21 +VTT_CPU_PWRGD
- +0.8VS
- 22 +0.8VS_PWRGD
- 23 ALL_SYSTEM_PWRGD
- 24 PM_PCHPWROK
- 25 H_DRAM_PWRGD
- 26 H_CPUPWRGD
- 27 SVID
- +VCORE
- +VccGFX
- 28 VRM_PWRGD
- 29 PM_SYSPWROK
- 30 BUF_PLT_RST#



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